MINISTERIO DE CIENCIA E INNOVACIÓN

Cofinanciado por la Unión Europea

AGENCIA ESTATAL DE INVESTIGACIÓN

CURRICULUM VITAE (CVA)

IMPORTANT – The Curriculum Vitae cannot exceed 4 pages. Instructions to fill this document are available in the website.

CV date	12/07/2023

Part A. PERSONAL INFORMATION

First name	Juan Antonio		
Family name	Maestro de la Cuerda		
Gender	Male		
e-mail	juamaest@ucm.es		
Open Researcher and Contributor ID (ORCID)		0000-0001-7133-9026	

A.1. Current position

Position	Catedrático de Universidad		
Initial date	01/07/2021		
Institution	Universidad Complutense de Madrid		
Department/Center	Arquitectura de Computadores y Automática	Facultad de Informática	
Country	Spain	Teleph. number	913947617
Key words	Electronics, Reliability, Computer Systems, Processors		

A.2. Previous positions

Period	Position/Institution/Country/Interruption cause
2004-2021	Full Professor – Universidad Nebrija
2010-2014	Vice Rector for Research – Universidad Nebrija
2003-2004	Lecturer – Saint Louis University
2000-2003	R+D Project Manager – CHEP S.A.
1995-2000	Assistant Professor – Universidad Complutense de Madrid

A.3. Education

PhD, Licensed, Graduate	University/Country	Year
Ph.D. (Computer Engineering)	Universidad Complutense de Madrid	1999
M.Sc. (Physics)	Universidad Complutense de Madrid	1994

Part B. CV SUMMARY

Juan Antonio Maestro is currently a full professor at the Computer Architecture Department of Universidad Complutense de Madrid. For the past 18 years, his main research line has been the fault tolerance of digital circuits, especially in Space applications. This research work has covered different kinds of components: specific signal processing systems, memories (using different error correction codes) and computer architectures (as RISC-V).
As a result of this activity, he has co-authored 205 research publications. Of these, 144 are JCR journal papers, with the following quartile distribution: Q1= 38, Q2= 55, Q3= 43, Q4= 8. These papers have been published both in journals specialized in the fault tolerance field (as Microelectronics Reliability or IEEE Transactions on Device and Materials Reliability), as well as in generalist journals (as IEEE Transactions on Computers or IEEE Transactions on VLSI). Besides, he is the co-author of 61 publications in conferences, as the Design Automation Conference (DAC), Design, Automation and Test in Europe (DATE), RADECS, IEEE

International Online Test Symposium (IOLTS) or Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT).
Regarding the scientific metrics, he has an h-index of 25 and 2.465 citations (according to Scopus, as of July 12, 2023). He also has three 6-year research periods recognized by the CNEAI.
He has participated in 15 competitive research projects, being the Principal Investigator of 6 of them. These projects span a wide range, from those nationally funded (Spanish Research State Plan, Community of Madrid, CDTI) to those funded at the European level (H2020, European Space Agency). He has also participated in 5 contracts funded by companies. In the transference field, he is the co-author of 3 industrial patents.
Regarding training activities, he has advised 9 Doctoral Theses. Of these, three obtained the International Mention and another three the Outstanding Doctorate Award.
Finally, regarding international exposure, he usually collaborates with different foreign institutions, as the European Space Agency, and he was appointed Visiting Professor by Stanford University.

Part C. RELEVANT MERITS *(sorted by typology)*

C.1. Publications

1. L.A. Aranda, O. Ruano, F. Garcia-Herrero, J.A. Maestro, "ACME-2: Improving the Extraction of Essential Bits in Xilinx SRAM-based FPGAs", IEEE Transactions on Circuits and Systems II (ISSN: 1549-7747), Vol. 69, No 3, March 2022, pp. 1577-1581.
2. F. García-Herrero, G. McGuire, M.F. Flanagan, A. Sánchez-Macián, J.A. Maestro, "Decoding Algorithm for Quadruple-Error-Correcting Reed-Solomon Codes and its Derived Architectures", IEEE Transactions on Circuits and Systems II (ISSN: 1549-7747), Vol. 68, No 4, April 2021, pp. 1438-1442.
3. L. A. Aranda, A. Sánchez-Macián and J. A. Maestro, “An Algorithmic-based Fault Detection Technique for the 1D Discrete Cosine Transform”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 5, May 2020, pp. 1336-1340.
4. A. Ramos, R. González-Toral, P. Reviriego, J.A. Maestro, "An ALU protection methodology for soft processors on SRAM-based FPGAs", IEEE Transactions on Computers (ISSN: 0018-9340), Vol. 68, No 9, September 2019, pp. 1404–1410.
5. A. Ullah, P. Reviriego, J.A. Maestro, "An efficient methodology for on-chip SEU injection in flip-flops for Xilinx FPGAs", IEEE Transactions on Nuclear Science (ISSN: 0018-9499), Vol. 65, No 4, April 2018, pp. 989-996.
6. A. Sánchez-Macián, P. Reviriego, J.A. Maestro, "Combined Modular Key and Data Error Protection for Content-Addressable Memories", IEEE Transactions on Computers (ISSN: 0018-9340), Vol. 66, No 6, June 2017, pp. 1085-1090.
7. M. Demirci, P. Reviriego, J.A. Maestro, "Unequal Error Protection Codes Derived from Double Error Correction Orthogonal Latin Square Codes", IEEE Transactions on Computers (ISSN: 0018-9340), Vol. 65, No 9, September 2016, pp. 2932-2938.
8. P. Reviriego, S. Pontarelli, A. Evans, J.A. Maestro, "A Class of SEC-DED-DAEC codes derived from Orthogonal Latin Square Codes", IEEE Transactions on Very Large Scale Integration (VLSI) Systems (ISSN: 1063-8210), Vol. 23, No 5, May 2015, pp. 968-972.
9. C. Argyrides, P. Reviriego, J.A. Maestro, "Using Single Error Correction Codes to Protect Against Isolated Defects and Soft Errors", IEEE Transactions on Reliability (ISSN: 0018-9529), Vol. 62, No 1, March 2013, pp. 238-243.
10. P. Reviriego, S. Pontarelli, J.A. Maestro, M. Ottavi, "A Method to Construct Low Delay Single Error Correction (SEC) Codes for Protecting Data Bits Only", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (ISSN: 0278-0070), Vol. 32, No 3, March 2013, pp. 479-483.

C.2. Conferences

1. L. Rodriguez-Soriano, N. Raveendran, F. Garcia-Herrero, B. Vasic, J.A. Maestro, "Evaluation of Quantum Generalized Belief Propagation Decoder", 3rd International Workshop on Quantum Resource Estimation (QRE2021), Valencia (Spain), June 19, 2021.
2. Y.M. Kuo, F. Garcia-Herrero, J.A. Maestro, "Versatile RISC-V ISA Galois Field arithmetic extension for cryptography and error-correction codes", Fifth Workshop on Computer Architecture Research with RISC-V (CARRV 2021), Valencia (Spain), June 17, 2021.
3. I. Wali, A. Sánchez-Macián, A. Ramos, J.A. Maestro "Analyzing the impact of the Operating System on the Reliability of a RISC-V FPGA Implementation", 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS2020), Glasgow (U.K.), November 23-25, 2020.
4. P. Reviriego, S. Liu, A. Sánchez-Macián, L. Xiao, J. A. Maestro, "Reduction of Parity Overhead in a Subset of Orthogonal Latin Square Codes", Design of Circuits and Integrated Systems Conference (DCIS2020), Segovia (Spain), November 18-20, 2020.
5. L.A. Aranda, P. Reviriego, J.A. Maestro, "Design Placement Guidelines for Single Event Upset (SEU) Minimization in SRAM-based FPGAs", Design of Circuits and Integrated Systems Conference (DCIS2017), Barcelona (Spain), November 22-24, 2017.
6. L.A. Aranda, P. Reviriego, J.A. Maestro, "A Fault-Tolerant Implementation of the Median Filter", Proc. of the RADECS 2016 conference, Bremen (Germany), September 19-23, 2016.
7. Z. Gao, P. Reviriego, J.A. Maestro, "Efficient Fault Tolerant Parallel Matrix-Vector Multiplications", Proc. of the IEEE International Online Test Symposium (IOLTS'16), Sant Feliu de Guixols (Spain), July 4-6, 2016, pp. 25-26.
8. P. Reviriego, S. Pontarelli, J.A. Maestro, M. Ottavi, "A Method to Protect Bloom Filters from Soft Errors", 28th IEEE Symp. Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2015), Amherst, MA (USA), October 12-14, 2015, pp. 80-84.
9. A.B. Boruzdina, A.V. Ulanova, A.G. Petrov, V.A. Telets, P. Reviriego, J.A. Maestro, "Verification of SRAM MCUs calculation technique for experiment time optimization", Proc. of the RADECS 2013 conference, Oxford (U.K.), September 23-27, 2013, pp. 1-4.
10. A. Sánchez-Macián, P. Reviriego, J.A. Maestro, "Modeling Reliability of Memories Protected with Error Correction Codes with RIIF", Proc. of the RIIF DATE 2013 Workshop, Grenoble (France), March 18-22, 2013.

C.3. Research projects

1. Project title: "Introduction of fault-tolerant concepts for RISC-V in space applications"
   Funding entity: European Space Agency (ESA)
   Participants: Universidad Antonio de Nebrija, Cobham Gaisler AB and QinetiQ Space NV.
   Duration, from: 05/2018 to: 10/2019
   Amount: 67.334 EUR
   Principal investigator: Juan Antonio Maestro de la Cuerda.

2. Project title: " Diseño, implementación y experimentación de técnicas de tolerancia a fallos para sistemas multi-procesador en aplicaciones espaciales embarcadas" (ESP2014-54505-C2-1-R).
   Funding entity: Ministerio de Economía y Competitividad – Plan Nacional de Espacio.
   Participants: Universidad Antonio de Nebrija, INTA.
   Duration, from: 01/2015 to: 12/2017
   Amount: 127.050 EUR
   Principal investigator: Juan Antonio Maestro de la Cuerda.

3. Project title: “Space Ethernet Physical Layer Transceiver (SEPHY)" (Proposal 640243 [COMPET-01-2014]).
   Funding entity: Comisión Europea – Horizonte 2020.
   Participants: Arquímea (coordinador), Universidad Antonio de Nebrija, Thales Alenia, Atmel, IHP y TTTech.
   Duration, from: 05/2015 to: 12/2018
   Amount: 359.350 EUR
   Principal investigator: Daniel González Gutiérrez (Arquímea)

4. Project title: “Diseño, simulación y experimentación con radiación sobre memorias y otros circuitos digitales complejos para aplicaciones espaciales embarcadas" (AYA2009-13300-C03-01).
   Funding entity: Ministerio de Ciencia e Innovación. – Plan Nacional de Espacio
   Participants: Universidad Antonio de Nebrija, Universidad Complutense de Madrid.
   Duration, from: 01/2010 to: 12/2012
   Amount: 118.000 EUR
   Principal investigator: Juan Antonio Maestro de la Cuerda.

C.4. Contracts, technological or transfer merits

1. Contract title: "New Protocol Semantics and Scheduling Primitives for Energy Efficiency: Burst Coalescing at the Link and Application Layers"
   Type: Google Research Award
   Funding entity: Google Inc
   Participants: Universidad Antonio de Nebrija/Universidad de South Florida
   Duration, from: 15/12/2011 to: 15/12/2012

2. Inventors: Juan Antonio Maestro, Pilar Reyes, Oscar Ruano, Pedro Reviriego
   Title: “Filtro de media móvil y método para la detección y corrección de errores utilizando paridad bidimensional”
   Application no.: P200930207 Country: Spain
   Date: 26-01-2011
   Entity: Universidad Antonio de Nebrija, Universidad Carlos III de Madrid

3. Inventors: Juan Antonio Maestro, Pilar Reyes, Oscar Ruano, Pedro Reviriego
   Title: “Método y filtro de media móvil para la detección y corrección de errores por medio de un filtro diezmado”
   Application no.: P200930205 Country: Spain
   Date: 16-05-2011
   Entity: Universidad Antonio de Nebrija, Universidad Carlos III de Madrid