MINISTERIO
DE CIENCIA, INNOVACIÓN
Y UNIVERSIDADES

CURRICULUM VITAE

CV date	12 Oct 2023

Part A. PERSONAL INFORMATION

First and Family name	Daniel Ángel Chaver Martínez		
Researcher numbers		Orcid code	https://orcid.org/0000-0002-1815-6412

Current position

Name of University/Institution	Complutense University of Madrid			
Department	Computer Architecture and Automation			
Address and Country	Office 236 at Physics Faculty, Ciudad Universitaria, 28040 Madrid, Spain			
Phone number	913944105	E-mail	dani02@ucm.es	
Current position	Associate Professor		From	20.01.2012
Espec. cód. UNESCO	330406			
Keywords	Processor Design, RISC-V, Microarchitecture			

Education

PhD	University	Year
Computer Science	Complutense University of Madrid	2006

JCR articles, h Index, thesis supervised…

Number of six-year periods with Positive Evaluation granted by the “Spanish Research Evaluation Commission (CNEAI)”: 3 (Last period: from 2014 to 2019).

JCR publications: 14

Ph.D. thesis advised: 3

Citations: 590 h-index: 15 Source for citations and h-index: Google Scholar

Part B. CV SUMMARY *(max. 3500 characters, including spaces)*

I obtained the M.Sc. degree in Physics from University of Santiago de Compostela in 1998, and the M.Sc. degree in Electronics Engineering and the Ph.D. degree in Computer Science from the University Complutense of Madrid (UCM) in 2000 and 2006, respectively. Currently I serve as an Associate Professor within the Computer Architecture and Automation Department at UCM.

I joined the Computer Architecture and Automation department at UCM in 2000. Since then, I have continuously participated in competitive projects related to the computer architecture field. Notably, my research interests include processor design (including energy-aware design), microarchitecture and efficient memory management. As a result of my research activity my scientific production includes 15 papers published in international journals with JCR impact factor (as *IEEE Micro*, *IEEE Transactions on Computers*, *Journal of Parallel and Distributed Computing* or *The Computer Journal*) more than 15 papers published in conferences of highly recognized prestige (as *IPDPS*, HiPC, *MICRO*, *SIGMETRICS*, *ISLPED*, *ICCD, SAC* or *DATE*) and 1 patent held by MIPS Tech. Inc.

Since 2002 I have collaborated with the research group headed by Prof. Michael C. Huang at University of Rochester (USA), with the Univerisy of San Luis at Argentina, and, in the recent years, with the Computer Architecture group (GaZ) of the University of Zaragoza (Spain) and with the companies Imagination and MIPS in different projects.

I have taught many courses related to Computer Science, Physics, Electronics Engineering and Communications Engineering since 2000, both in BSc and MSc degrees, and both at the University Complutense of Madrid and at some foreign universities.

I was the Academic Secretary of the Dept. of Computer Architecture and System Engineering since 2006 to 2015, the Vice-Director of the Dept. of Computer Architecture and System Engineering since 2016 to 2018 and the Vice-Dean of External Relations and Research at the School of Computer Science since 2018 to 2022.

Part C. RELEVANT MERITS

Publications (including books) (max. 10)

1. Sarah L Harris, Daniel Chaver, Luis Piñuel, Olof Kindgren, Robert CW Owen: RVfpga: Computer Architecture Course and MOOC Using a RISC-V SoC Targeted to an FPGA and Simulation. (2023). 2023 ASEE Annual Conference & Exposition, Baltimore, Maryland. https://peer.asee.org/44172.

2. Sarah L Harris, Daniel Chaver, Luis Piñuel, JI Gomez-Perez, M Hamza Liaqat, Zubair L Kakakhel, Olof Kindgren, Robert Owen: RVfpga: Using a risc-v core targeted to an fpga in computer architecture education. (2021). 31st International Conference on Field-Programmable Logic and Applications. doi: 10.1109/FPL53798.2021.00032.

3. Rodríguez-Rodríguez, R., Díaz, J., Castro, F., Ibáñez, P., Chaver, D., Viñals, V., Sáez, J.C., Piñuel, L., Prieto, M., Monreal, T., Llabería, J. M.: Reuse Detector: Improving the Management of STT-RAM SLLCs. The Computer Journal, 61(6): 856-880 (2018). ISSN: 0010-4620. doi: 10.1093/comjnl/bxx099.

4. Sarah L Harris, David M Harris, Daniel Chaver, Robert Owen, Zubair L Kakakhel, Enrique Sedano, Yuri Panchul, Bruce Ableidinger: MIPSfpga: using a commercial MIPS soft-core in computer architecture education. IET Circuits, Devices & Systems (2017). ISSN: 1751-858X. doi: 10.1049/iet-cds.2016.0383.

5. Sáez, J. C., Pousa, A., Castro, F. Chaver, D., Prieto, M.:Towards completely fair scheduling on asymmetric single-ISA multicore processors. Journal of Parallel and Distributed Computing. 102: 115-131 (2017). ISSN: 0743-7315. doi: 10.1016/j.jpdc.2016.12.011.

6. Rodríguez-Rodríguez, R., Castro, F., Chaver, D., Gonzalez-Alberquilla, R., Pinuel, L., Tirado, F.: Write-Aware Replacement Policies for PCM-Based Systems, The Computer Journal, 58(9): 2000-2025 (2015). ISSN: 0010-4620. DOI: 10.1093/comjnl/bxu104.

7. Castro, F., Noor, R., Garg, A., Chaver, D., Huang, M. C., Pinuel, L., Prieto, M., Tirado, F.: Replacing Associative Load Queues: A Timing Centric Approach. IEEE Transactions on Computers, 58(4): 496 – 511, (2009). ISSN 0018-9340. doi: 10.1109/TC.2008.146.

8. Castro, F., Pinuel, L., Chaver, D., Prieto, M., Huang, M. C., Tirado, F.: DMDC: Delayed Memory Dependence Checking through Age-Based Filtering, IEEE/ACM International Symposium on Microarchitecture (MICRO), Orlando, FL, USA: 297- 308, (2006). ISSN: 1072-4451 - Print ISBN: 0-7695-2732-9. doi: 10.1109/MICRO.2006.21.

9. Huang, M. C., Chaver, D., Pinuel, L., Prieto, M., Tirado, F.: Customizing the Branch Predictor to Reduce Complexity and Energy Consumption, IEEE Micro Magazine, (2003) ISSN: 0272-1732. DOI: 10.1109/MM.2003.1240209.

10. D. Chaver, L. Piñuel, M. Prieto, F. Tirado: Parallel Wavelet Transform for Large Scale Image Processing, Proceedings of the IEEE International Parallel and Distributed Processing Symposium (IEEE-IPDPS-02), 1-6, (2002). ISBN: 0-7695-1573-8. doi: 10.1109/IPDPS.2002.1015472.

Research projects and grants (max. 5)

1. Title: Architecture Specialization from arIthmetical and MemOry perspectiVes (ASIMOV)
   Funding entity: Ministerio de Ciencia e Innovación (PID2021-123041OB-I00)
   Principal Investigator: Alberto A. del Barrio / José Luis Imaña
   Participating entities: Complutense University of Madrid
   Starting date: 01.09.2022 Ending date: 31.08.2025
   Role: Investigator
   Project amount: 132,979 €

2. Title: HETEROGENEIDAD Y ESPECIALIZACION EN LA ERA POST-MOORE
   Funding entity: Ministerio de Ciencia, Innovación y Universidades (RTI2018-093684-B-I00)
   Principal Investigator: Manuel Prieto Matías / Luis Piñuel Moreno
   Participating entities: Complutense University of Madrid
   Starting date: 01.01.2019 Ending date: 12.31.2021
   Role: Investigator
   Project amount: 300,927 €

3. Title: Efficient heterogeneous computing: from the processor to the datacenter (COPHERNICO)
   Funding entity: MINECO (TIN2015-65277-R)
   Principal Investigator: Manuel Prieto Matías / Luis Piñuel Moreno
   Participating entities: Complutense University of Madrid
   Starting date: 01.01.2016 Ending date: 12.31.2018
   Role: Investigator
   Project amount: 371,470 €

4. Title: Architectures and emerging technologies. Energy efficiency through heterogenety
   Funding entity: MEC (TIN2012-32180)
   Principal Investigator: Manuel Prieto Matías
   Participating entities: Complutense University of Madrid
   Starting date: 01.01.2013 Ending date: 12.31.2015
   Role: Investigator
   Project amount: 219,620 €

5. Title: Hardware/software architecture for high-performance systems II
   Funding entity: National Science Agency (TIN2008-00508)
   Principal Investigator: Francisco Tirado Fernández
   Participating entities: Complutense University of Madrid
   Starting date: 01.01.2009 Ending date: 06.30.2015
   Role: Investigator
   Project amount: 1,217,260 €

Contracts

1. Title: Development of MIPSfpga v2.0
   Funding entity: Imagination Technologies
   Principal Investigator: Daniel Chaver Martinez
   Participating entities: Complutense University of Madrid, Imagination Technologies and University of Nevada Las Vegas
   Starting date: 11.14.2016 Ending date: 05.14.2017
   Project amount: 4,000 €

2. Title: Development of RISC-Vfpga
   Funding entity: Imagination Technologies
   Principal Investigator: Daniel Chaver Martinez
   Participating entities: Complutense University of Madrid, Imagination Technologies and University of Nevada Las Vegas
   Starting date: 01.04.2020 Ending date: 31.12.2023
   Project amount: 100,719 €

Patents

1. Authors: Andrew David Webber, Daniel Ángel Chaver Martínez, Enrique Sedano Algarabel
   Proprietor: WAVE COMPUTING LIQUIDATING TRUST, CALIFORNIA, US
   Title: Fetching instructions in an instruction fetch unit
   (https://patents.google.com/patent/US20170364357A1/en)
   Patent Number: US10372453B2

Ph.D. thesis advised

1. Title: Mecanismos para la gestion de accesos a memoria fuera de orden
   Student: Fernando Castro Rodríguez
   University: UCM
   Advisors: Manuel Prieto, Luis Piñuel and Daniel Chaver
   Date: 9 de junio de 2008
   Grade: Sobresaliente cum laude

2. Title: Mecanismos para filtrado de accesos a la lsq y a la cache de datos en una arquitectura x86
   Student: Rubén Gerardo Apolloni
   University: Universidad Nacional de San Luis
   Advisors: Francisco Tirado and Daniel Chaver
   Date: 15 de diciembre de 2011
   Grade: Sobresaliente cum laude

3. Title: Mecanismos de gestión de escrituras en sistemas con tecnologías de memoria no volátiles
   Student: Roberto Alonso Rodríguez Rodríguez
   University: UCM
   Advisors: Fernando Castro and Daniel Chaver
   Date: 18 de noviembre de 2016
   Grade: Sobresaliente cum laude

Researching stays

1. MIPS - Imagination Technologies Ltd (London, UK), July 2015 to February 2016.
2. Universidad de San Luis (Argentina), November 2010.
3. Universidad de Rochester (NY, USA), 5 months along years 2003 and 2005.
4. Universidad de Urbana Champaign (IL, USA), July to August 2002.