MINISTERIO DE CIENCIA, INNOVACIÓN Y UNIVERSIDADES

CURRICULUM VITAE (maximum 4 pages)

Part A. PERSONAL INFORMATION

CV date	09.25.2018

First and Family name	Fernando Castro Rodriguez		
Social Security, Passport, ID number	76710480Y	Age	41
Researcher numbers	Researcher ID	G-8704-2015	
	Orcid code	0000-0002-2773-3023	

A.1. Current position

Name of University/Institution	Complutense University of Madrid			
Department	Computer Architecture and Automation			
Address and Country	Physics Faculty, Complutense University of Madrid, Ciudad Universitaria, Plaza de las Ciencias, 28040 Madrid, Spain			
Phone number	913944892	E-mail	fcastror@ucm.es	
Current position	Associate Professor		From	10.01.2013
Espec. cód. UNESCO	330406			
Keywords	Processor design, emerging memory technologies, system software			

A.2. Education

PhD	University	Year
Computer Science	Complutense University of Madrid	2008

A.3. JCR articles, h Index, thesis supervised…

Number of six-year periods with Positive Evaluation granted by the "Spanish Research Evaluation Commission (CNEAI)": Two. Last period: from 2012 to 2017.
JCR Q1 publications: 1 JCR Q2 publications: 2
Ph.D. thesis advised in the last 10 years: 1
Citations: 187 Average citations/year (2013-2017): 26
h-index: 8
Source for citations and h-index: Google Scholar

Part B. CV SUMMARY *(max. 3500 characters, including spaces)*

I obtained the MS degree in Physics from University of Santiago de Compostela in 2000, and the MS degree in Electrical Engineering and the Ph.D. degree in Computer Science from the Complutense University of Madrid (UCM) in 2004 and 2008, respectively. Currently I serve as Associate Professor within the Computer Architecture and Automation department, at UCM, also performing management tasks derived from my Academic Secretary charge.

I joined the Computer Architecture and Automation department at UCM in 2003 thorough an FPI grant. Since 2003, I have continuously participated in competitive projects related to the computer architecture field. Notably, my research interests include energy-aware processor design, efficient memory management (including emerging non-volatile memory technologies) and OS scheduling on heterogeneous multiprocessors. My very recent activities also focused on the software engineering, exploring new tools aiming to improve the classroom teaching.

As a result of my research activity developed since 2006 my scientific production include 13 papers published in international journals with JCR impact factor (as *IEEE Transactions on Computers*, *Journal of Parallel and Distributed Computing* or *The Computer Journal*) and other 8 papers published in the proceedings of very recognized prestige (as *MICRO*, *SIGMETRICS*, *ISLPED*, *ICCD, SAC* or *DATE*).

Also, since 2004 I have collaborated with the research group headed by Prof. Michael C. Huang at University of Rochester (USA), and in the recent years with the Computer Architecture group (GaZ) of the University of Zaragoza (Spain).

Part C. RELEVANT MERITS

C.1. Publications (including books)

1. Rodríguez-Rodríguez, R., Díaz, J., Castro, F., Ibáñez, P., Chaver, D., Viñals, V., Sáez, J.C., Piñuel, L., Prieto, M., Monreal, T., Llabería, J. M.: Reuse Detector: Improving the Management of STT-RAM SLLCs. The Computer Journal, 61(6): 856-880 (2018). ISSN: 0010-4620. doi: 10.1093/comjnl/bxx099.

2. Sáez, J. C., Pousa, A., Castro, F. Chaver, D., Prieto, M.:Towards completely fair scheduling on asymmetric single-ISA multicore processors. Journal of Parallel and Distributed Computing. 102: 115-131 (2017). ISSN: 0743-7315. doi: 10.1016/j.jpdc.2016.12.011.

3. Sáez, J. C., Pousa, A., Rodríguez-Rodríguez, R., Castro, F., Prieto, M.: PMCTrack: Delivering Performance Monitoring Counter Support to the OS Scheduler. The Computer Journal, 60(1): 60-85 (2017). ISSN: 0010-4620. doi: 10.1093/comjnl/bxw065.

4. Rodríguez-Rodríguez, R., Castro, F., Chaver, D., Gonzalez-Alberquilla, R., Pinuel, L., Tirado, F.: Write-Aware Replacement Policies for PCM-Based Systems, The Computer Journal, 58(9): 2000-2025 (2015). ISSN: 0010-4620. DOI: 10.1093/comjnl/bxu104.

5. Sáez, J. C., Castro, F., Chaver, D., Prieto, M.: Delivering fairness and priority enforcement on asymmetric multicore systems via OS scheduling, ACM SIGMETRICS, Pittsburgh, PA, USA: 343-344, (2013). ISBN: 978-1-4503-1900-3. doi: 10.1145/2465529.2465532.

6. Rodríguez-Rodríguez, R., Castro, F., Chaver, D., Pinuel, L., Tirado, F.: Reducing writes in phase-change memory environments by using efficient cache replacement policies, Design, Automation and Test in Europe Conference & Exhibition (DATE), Grenoble, France: 93-96, (2013). ISBN: 978-1-4503-2153-2. doi: 10.7873/DATE.2013.033.

7. Gonzalez-Alberquilla, R., Castro, F., Pinuel, L., Tirado, F.: Stack filter: Reducing L1 data cache power consumption, Journal of Systems Architecture, 56(12): 685-695, (2010). ISSN: 1383-7621. doi: 10.1016/j.sysarc.2010.10.002.

8. Castro, F., Noor, R., Garg, A., Chaver, D., Huang, M. C., Pinuel, L., Prieto, M., Tirado, F.: Replacing Associative Load Queues: A Timing Centric Approach. IEEE Transactions on Computers, 58(4): 496 – 511, (2009). ISSN 0018-9340. doi: 10.1109/TC.2008.146.

9. Castro, F., Chaver, D., Pinuel, L., Prieto, M., Tirado, F.: Using age registers for a simple load-store queue filtering, Journal of Systems Architecture, 55(2): 79-89, (2009). ISSN: 1383-7621. doi: 10.1016/j.sysarc.2008.09.005.

10. Castro, F., Pinuel, L., Chaver, D., Prieto, M., Huang, M. C., Tirado, F.: DMDC: Delayed Memory Dependence Checking through Age-Based Filtering, IEEE/ACM International Symposium on Microarchitecture (MICRO), Orlando, FL, USA: 297- 308, (2006). ISSN: 1072-4451 - Print ISBN: 0-7695-2732-9. doi: 10.1109/MICRO.2006.21.

C.2. Research projects and grants

1. Title: Efficient heterogeneous computing: from the processor to the datacenter (COPHERNICO)
Funding entity: MINECO (TIN2015-65277-R)
Principal Investigator: Manuel Prieto Matías / Luis Piñuel Moreno

Participating entities: Complutense University of Madrid
Starting date: 01.01.2016 Ending date: 12.31.2018
Role: Investigator
Project amount: 371,470 €

2. Title: Architectures and emerging technologies. Energy efficiency through heterogenety
Funding entity: MEC (TIN2012-32180)
Principal Investigator: Manuel Prieto Matías
Participating entities: Complutense University of Madrid
Starting date: 01.01.2013 Ending date: 12.31.2015
Role: Investigator
Project amount: 219,620 €

3. Title: Hardware/software architecture for high-performance systems II
Funding entity: National Science Agency (TIN2008-00508)
Principal Investigator: Francisco Tirado Fernández
Participating entities: Complutense University of Madrid
Starting date: 01.01.2009 Ending date: 06.30.2015
Role: Investigator
Project amount: 1,217,260 €

4. Title: Hardware/software architecture for high-performance systems
Funding entity: National Science Agency (TIN2005-05619)
Principal Investigator: Francisco Tirado Fernández
Participating entities: Complutense University of Madrid
Starting date: 01.01.2006 Ending date: 12.31.2008
Role: Investigator
Project amount: 596,190 €

5. Title: Hardware/software technology for high-performance systems
Funding entity: National Science Agency (TIC2002-00750)
Principal Investigator: Francisco Tirado Fernández
Participating entities: Complutense University of Madrid
Starting date: 01.01.2003 Ending date: 12.31.2005
Role: Investigator
Project amount: 511,787 €

C.3. Contracts

1. Title: Development of MIPSfpga v2.0
   Funding entity: Imagination Technologies
   Principal Investigator: Daniel Chaver Martinez
   Participating entities: Complutense University of Madrid
   Starting date: 11.14.2016 Ending date: 05.14.2017
   Role: Investigator
   Project amount: 4,000 €

2. Title: Optimization of a HW/SW plataform for the development of services for a satellital device over an imperative programming language
   Funding entity: SATLINK S.L.
   Principal Investigator: Luis Piñuel Moreno
   Participating entities: Complutense University of Madrid
   Starting date: 12.10.2014 Ending date: 11.10.2015
   Role: Investigator
   Project amount: 77,082 €

3. Title: HW/SW Plataform for the development of services for a satellital device over an imperative programming language

Funding entity: SATLINK S.L. (C-2649)
Principal Investigator: Luis Piñuel Moreno
Participating entities: Complutense University of Madrid
Starting date: 10.16.2013 Ending date: 09.16.2014
Role: Investigator
Project amount: 62,985 €

4. Title: Development of an FTP server for data transfer from a Flash-memories board and evaluation of the effort required for the target system
Funding entity: INDRA S.A. (C-2618)
Principal Investigator: Luis Piñuel Moreno
Participating entities: Complutense University of Madrid
Starting date: 07.20.2011 Ending date: 09.26.2011
Role: Investigator
Project amount: 31,500 €

C.4. Patents

C.5 Ph.D. thesis advised

Title: Write management mechanisms for systems with non-volatile memory technologies
Student: Roberto Alonso Rodríguez Rodríguez
Advisors: Fernando Castro Rodriguez and Daniel Chaver Martinez
Date: 11.18.2016
Grade: Sobresaliente cum laude

C.6. Researching stays

Organization: University of Rochester (NY, USA).
Group: Electrical & Computer Engineering.
2 Stays:
- 2 months (August-September 2004).
- 1 month (July 2005).

Contact: Michael C. Huang.

C.7. Grants

FPI (Predoctoral researching grant) of Spanish Education Ministry associated to the project “Hardware/software technology for high-performance systems”, granted in a competitve process. From 05.01.2003 to 11.14.2005.

C.8 Collaborations in journal and conferences

- Reviewer of IEEE Transacactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Parallel and Distributed Systems, Microprocessors & Microsystems Journal, Parallel Computing, Journal of Circuits, Systems and Computers.
- Reviewer of SAMOS, CODES+ISSS, EuroPar, PDP, PACT.

C.9 Other

- Spanish Credential for becoming an Associate Professor (tenured, civil servant). March 2015.
- Participation in the development of the "OpenIRS-UCM" software, adopted by the Complutense Univerity of Madrid in recent years to perform the evaluation of teaching quality within DOCENTIA program.
- Member of the European Network on High Performance and Embedded Architecture and Compilation (Hipeac) and the Spanish CAPAP-H network