CV Date	11/10/2023

Part A. PERSONAL INFORMATION

First Name *	Alberto Antonio		
Family Name *	Del Barrio García		
Sex *	Male	Date of Birth *	21/03/1983
ID number Social Security, Passport *			
URL Web	https://artecs.dacya.ucm.es/people/?uid=alberto-a-del-barrio-2		
Email Address *	abarriog@ucm.es		
Open Researcher and Contributor ID (ORCID)*	0000-0002-6769-1200		

A.1. Current position

Job Title	Profesor Titular de Universidad (Associate Prof., tenured, civil-servant)		
Starting date	2021		
Institution	Universidad Complutense de Madrid		
Department / Centre	Arquitectura de Computadores y Automática / Facultad de Informática		
Country	Spain	Phone Number	00913944372
Keywords	Architecture of computers; Design of digital integrated circuits		

A.2. Prior positions (including interruptions)

Period	Job Title / Name of Employer / Country
2020 - 2021	Profesor Contratado Doctor / Universidad Complutense de Madrid
2017 - 2020	Profesor Contratado Doctor interino / Universidad Complutense de Madrid
2017 - 2017	Profesor Visitante / Universidad Complutense de Madrid
2012 - 2017	Profesor Ayudante Doctor / Universidad Complutense de Madrid
2009 - 2012	Profesor Ayudante / Universidad Complutense de Madrid
2007 - 2009	Becario FPU / Universidad Complutense de Madrid
2007 - 2007	Becario de Colaboración (Máster) / Universidad Complutense de Madrid
2006 - 2006	Contratado por proyecto (TIN2005-05619) / Universidad Complutense de Madrid

A.3. Education

Degree/Master/PhD	University / Country	Year
Programa Oficial de Doctorado en Ingeniería Informática	Universidad Complutense de Madrid	2011
Máster Universitario en Investigación en Informática	Universidad Complutense de Madrid	2007
Ingeniero en Informática	Universidad Complutense de Madrid	2006

Part B. CV SUMMARY

In 2011 I got my PhD in Computer Science, at Universidad Complutense de Madrid. I have been Teaching Assistant from January 2009 to December 2011, an Assistant Professor from January 2012 to January 2017, a Visiting Professor since January 2017 to July 2017, tenured Associate Professor since July 2017, and since June 2021 I am a civil-servant too. Since December 2020 I am the Academic Secretary of my department.

During all these years I have been teaching BS and MS subjects such as: Architecture and Programming of Quantum Computers, Distributed Embedded Systems, Computer Architecture or Computer Networks. I have been the PI of three Teaching Innovation Projects at UCM and participated in another five. Also I have acted as the UCM coordinator of the K-R hub UNA Europa Seed Funding project.

As a researcher I have developed my expertise in the Design Automation and the Computer Arithmetic areas, always associated to the ArTeCS group in the UCM. My most important contributions at the design level can be found at https://github.com/albertodbg/. Nowadays I am widening my knowledge by applying these ideas in the Neural Networks, Analog and Quantum Computing fields. Within the ArTeCS group, I have continuously been participating in projects of the National Plan since I joined as a PhD student in 2007. I am author or co-author of more than 80 international publications: IEEE Trans. On Emerging Topics in Computing (3), IEEE Trans. On Computers (2), IEEE Trans. On CAS-I (2), IEEE Trans. On CAS-II (2), IEEE Trans. On CAD (3), IEEE Access (2), DSP (3), IEEE Design & Test (1), ACM TECS (1), Journal of Supercomputing (1), Microelectonics Journal (1), Integration (1), DATE (4), ASP-DAC (1), ICCD (3), ARITH (2), ISCAS (1), ASAP (1), DSD (1) among others. Overall, 32 researching journals indexed in the Journal Citation Report, out of which 25 belong to the first or second quartile.

I am a frequent reviewer in several relevant conferences and journals: DAC, ICCAD, DATE (regular TPC member), FCCM, CODES+ISSS, SummerSim, IEEE Trans. On Emerging Topics in Computing, IEEE Trans. On Computers, IEEE Trans. On CAD, IEEE Trans. On CAS-I, DSP. Furthermore, I have performed researching stays in several top universities, funded by competitive grants: Northwestern University (2008, FPU grant support), University of California at Irvine (2012, Del Amo grant support), University of California at Los Angeles (2013, Hipeac Collaboration grant support). Since 2019 I have become an IEEE Senior Member and since 2020 an ACM Senior Member.

I have supervised 3 PhD thesis and currently I am advising another 7. In addition, I have been positively evaluated in two six-year period research by “Spanish Research Evaluation Commission" (CNEAI), namely: 2008-2013 and 2014-2019, which is the maximum that I am allowed.

Currently I am leading the ASIMOV project, funded by the Spanish MICINN with 133k€. The main objectives of this project are to optimize kernels from the arithmetic and memory point of view, as well as exploring non-conventional approaches as quantum or analog computing. In the past, I also led the PARNASO project, funded by Fundación BBVA with 40k€ to develop a RISC- V core supporting the novel posit format in order to optimize the Neural Networks training stage. Some of the outcomes can be found at https://github.com/artecs-group/PERCIVAL. Furthermore, I have been awarded by the IonQ Research Credits Program with 10,000 USD in 2021 and by Azure Microsoft in 2022 to test their trapped ion-based quantum computers/platforms.

At the transfer level, I have participated or am participating in a total of 4 contracts with both national and international companies, consisting of an overall budget of 100k€. Among these companies we can highlight IBM, Imagination Technologies or Indra Sistemas.

Finally, here are some statistics about my research:

Number of six-year periods with Positive Evaluation granted by the "Spanish Research Evaluation Commission (CNEAI)": Two. Last period: from 2014 to 2019.
Supervised thesis in the last 10 years: 3

- Google Scholar: 905 citations, average citations/year (2018-2023): 121.2, h-index: 16.
- Scopus: 501 citations, average citations/year (2018-2023): 55.3, h-index: 13.
- Research Gate: 671 citations; average citations/year (2018-2023): 91.5; research interest index: 480.2; 44 recommendations; 30,737 reads, h-index: 15.

Part C. MOST RELEVANT CONTRIBUTIONS

C.1. Publications (selected 12)

1 **Scientific paper.** R. Murillo, **A. A. D. Barrio**, G. Botella and C. Pilato, "Generating Posit-Based Accelerators With High-Level Synthesis," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 70, no. 10, pp. 4040-4052, Oct. 2023.
JIF(JCR-2022): 5.1 (rank: 68/275). ISSN: 2168-6750. doi: 10.1109/TCSI.2023.3299009

2 **Scientific paper.** R. Murillo, J. Hormigo, **A. A. D. Barrio** and G. Botella, "HUB Meets Posit: Arithmetic Units Implementation," in IEEE Transactions on Circuits and Systems II: Express Briefs.
JIF(JCR-2022): 4.4 (rank: 84/275). ISSN: 2168-6750. doi: 10.1109/TCSII.2023.3307488

3 **Scientific paper.** Gines Carrascal, Guillermo Botella, **Alberto del Barrio** and David Kremer. EPJ Quantum Technol., 10 1 (2023) 13.
JIF(JCR-2022): 5.3 (rank: 16/100). ISSN: 2662-4400. doi: 10.1140/epjqt/s40507-023-00171-4

4 **Scientific paper.** R. Murillo, **A. A. Del Barrio** and G. Botella, "A Suite of Division Algorithms for Posit Arithmetic," 2023 IEEE 34th International Conference on Application-specific Systems, Architectures and Processors (ASAP), Porto, Portugal, 2023, pp. 41-44, doi: 10.1109/ASAP57973.2023.00020.

5 **Scientific paper.** D. Mallasén, R. Murillo, **A. A. D. Barrio**, G. Botella, L. Piñuel and M. Prieto-Matias, "PERCIVAL: Open-Source Posit RISC-V Core With Quire Capability," in IEEE Transactions on Emerging Topics in Computing, vol. 10, no. 3, pp. 1241-1252, 1 July-Sept. 2022.
JIF(JCR-2022): 5.9 (rank: 35/158). ISSN: 2168-6750. doi: 10.1109/TETC.2022.3187199

6 **Scientific paper.** R. Murillo, **A. A. Del Barrio**, G. Botella, M. S. Kim, H. Kim and N. Bagherzadeh, "PLAM: A Posit Logarithm-Approximate Multiplier," in IEEE Transactions on Emerging Topics in Computing, vol. 10, no. 4, pp. 2079-2085, 1 Oct.-Dec. 2022.
JIF(JCR-2022): 5.9 (rank: 35/158). ISSN: 2168-6750. doi: 10.1109/TETC.2021.3109127

7 **Scientific paper.** M. S. Kim, **A. A. Del Barrio**, H. Kim and N. Bagherzadeh, "The Effects of Approximate Multiplication on Convolutional Neural Networks," in IEEE Transactions on Emerging Topics in Computing, vol. 10, no. 2, pp. 904-916, 1 April-June 2022.
JIF(JCR-2022): 5.9 (rank: 35/158). ISSN: 2168-6750. doi: 10.1109/TETC.2021.3050989

8 **Scientific book or monograph.** Murillo, Raúl; Mallasén, David; **Del Barrio, Alberto A;** Botella, Guillermo. Energy-Efficient MAC Units for Fused Posit Arithmetic. 2021 IEEE 39th International Conference on Computer Design (ICCD), 2021, pp. 138-145.
Clase GGS 2. doi: 10.1109/ICCD53106.2021.00032.

9 **Scientific paper.** García Moreno, Daniel; **Del Barrio, Alberto A**; Botella, Guillermo; Hasler, Jennifer. 2021. A Cluster of FPAAs to Recognize Images using Neural Networks IEEE Transactions on Circuits and Systems II: Express Briefs. IEEE. 68-11, pp.3391-3395.
JIF(JCR-2021): 3.691 (rank: 100/276). ISSN: 1558-3791. doi: 10.1109/TCSII.2021.3077392

10 **Scientific paper.** Kim, MS; **Del Barrio, Alberto A**; Tavares, L; Hermida, R; Bagherzadeh, N. 2019. Efficient Mitchell's Approximate Log Multipliers for Convolutional Neural Networks IEEE Transactions on Computers. 68-5, pp.660-675.
JIF(JCR-2019): 2.711 (rank: 19/53). ISSN: 0018-9340. doi:10.1109/TC.2018.2880742.

11 **Scientific paper. Del Barrio, Alberto A**; Hermida, Román; Ogrenci-Memik, Seda. 2018. A combined arithmetic-high-level synthesis solution to deploy partial carry-save radix-8 booth multipliers in datapaths. IEEE Transactions on Circuits and Systems I: Regular Papers. IEEE. 66-2, pp.742-755.
JIF(JCR-2019): 3.318 (rank 74/266). ISSN: 1549-8328. doi:10.1109/TCSI.2018.2866172.

12 **Scientific paper. Del Barrio, Alberto A**; Hermida, Román; Ogrenci Memik, Seda. 2016. A Partial Carry-Save On-the-fly Correction Multispeculative Multiplier IEEE Transactions on Computers.
IF(JCR-2016): 2.916 (rank: 10/52). ISSN: 0018-9340. doi:10.1109/TC.2016.2529626.

Repositories related to the papers:

- https://github.com/albertodbg/vhdl-arithmetic
- https://github.com/albertodbg/log-arithmetic
- https://github.com/RaulMurillo/deep-pensieve
- https://github.com/artecs-group/PERCIVAL
- https://github.com/artecs-group/llvm-xposit
- https://github.com/artecs-group/Flo-Posit
- https://github.com/artecs-group/hub-posit

C.3. Research projects (selected 6)

1 **Project.** Architecture Specialization from arIthmetical and MemOry perspectiVes (ASIMOV). Ministerio de Ciencia e Innovación. **Alberto A. del Barrio** y José Luis Imaña. (Universidad Complutense de Madrid). 01/09/2022-31/08/2025. 132,979 €.

2 **Project**. PARNASO: Plataforma de Aceleración de Redes Neuronales profundas basadas en posits. Fundación BBVA. **Alberto A. del Barrio García.** (Universidad Complutense de Madrid). 30/09/2020-30/06/2022. 40,000 €.

3 **Project.** ConvergenciA Big dAta-Hpc: de Los sensores a las Aplicaciones (CABAHLA-CM). Comunidad de Madrid. José Francisco Tirado Fernández. (Universidad Complutense de Madrid). 01/01/2019-31/12/2022. 869,400 €.

4 **Project.** Heterogeneidad y especialización en la era post-Moore (cHIMERA). Ministerio de Ciencia e Innovación y Universidades. Manuel Prieto Matías. (Universidad Complutense de Madrid). 01/01/2019-31/12/2021. 300,927 €.

5 **Project.** Efficient heterogeneous computing: from the processor to the datacenter (COPHERNICO). Ministerio de Economía y Competitividad. Manuel Prieto Matías. (Universidad Complutense de Madrid). 01/01/2016-31/12/2018. 371,470 €.

6 **Project.** Detección tEmprana del deSarrollo tumoral mediante Computación de Altas pResTacionES (DESCARTES). BANCO SANTANDER, S.A.; Universidad Complutense de Madrid. Guillermo Botella Juan. (Universidad Complutense de Madrid). 22/12/2016-21/12/2018. 20,000 €.

C.4. Transfer

1 **Contract.** Desarrollo de RISC-Vfpga v3.0. Imagination Technologies. Daniel A. Chaver Martínez. 01/01/2020-31/12/2022. 70,000 €.

2 **Contract.** Aplicabilidad de la Computación Cuántica para Entornos Financieros IBM, S.A.. Guillermo Botella Juan. 20/07/2021-20/07/2022. 4,500 €.

3 **Contract.** Incorporación de un media-server a SATLINK PBX v2. Luis Piñuel Moreno. 15/06/2016-15/11/2016. 13,823€.

4 **Contract.** Diseño de SOC sobre FPGA basado en VHDL. Hortensia Mecha López. 23/10/2014-21/12/2014. 8,000€.