UNIVERSIDAD COMPLUTENSE MADRID

Facultad de Informática

ANUNCIO DE CONFERENCIA

POSGRADO

Semidynamics RISC-V IP Cores

Roger Espasa
Semydynamics

Facultad de Informática
Sala de Grados - miércoles 18 de octubre de 2023 - 13:00
Entrada libre hasta completar el aforo

Resumen:

In this conference, Roger Espasa (CEO & Founder of Semidynamics) will explain Semidynamics RISC-V Cores; Atrevido Out-of-Order core and Avipado In-Order core. Also he will present the two main own technologies, Semidynamics Out-of-Order Vector Unit and the advantages of Gazzillion Misses.

Sobre Roger Espasa:

Roger Espasa is the founder and CEO of Semidynamics, an IP supplier of two RISC-V cores, Avispado (in-order) and Atrevido (out-of-order) supporting the RISC-V vector extension and GazzillionTM misses, both targeted at HPC and Machine Learning. Prior to Semidynamics, Roger was at Broadcom working on an ARMV8 wide out-of-order core. (2014-2016). Previously, Roger worked at Intel (2002-2014) developing a vector extension for the x86 ISA, initially deployed in XeonPhi (Larrabee) which then became AVX-512. Roger also led the texture sampling unit for Larrabee. Roger then worked on Knight's Landing (14nm) and led the core for Knights Hill (10nm). Between 1999 and 2001 Roger worked for the Alpha Microprocessor Group on a vector extension to the Alpha architecture known as Tarantula. Roger got his PhD from UPC in 1997, has published over 40 peer-reviewed papers on Vector Architectures, Graphics/3D Architecture, Binary translation and optimization, Branch Prediction, and Media ISA Extensions and holds 9 patents with 41 international filings.