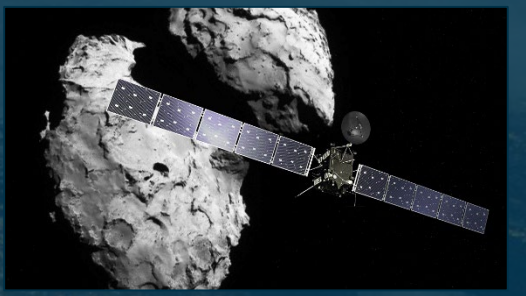
uElectronics on-going activities at ESA

To be presented at *Conferencias de Posgrado* – FdI (UCM) - Nov'22

Alberto Urbón Aguado – ESA on behalf of Telespazio
30/11/2022

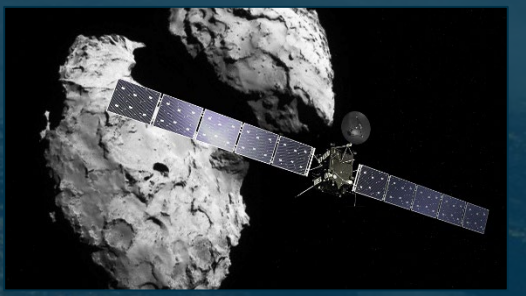
Outline

1. **Who?**
    1. ESA
    2. ESTEC
    3. TEC-EDM
2. **R+D activities**
    1. Rad-Hard European FPGAs: a new player in the market
    2. Upcoming IPs
    3. FPGAs On-board reliable reconfiguration
    4. RISC-V activities
    5. Others
3. **Working at/with ESA**
4. **Q&A**



Outline

1. Who?
    1. ESA



1.1 – Who? - ESA

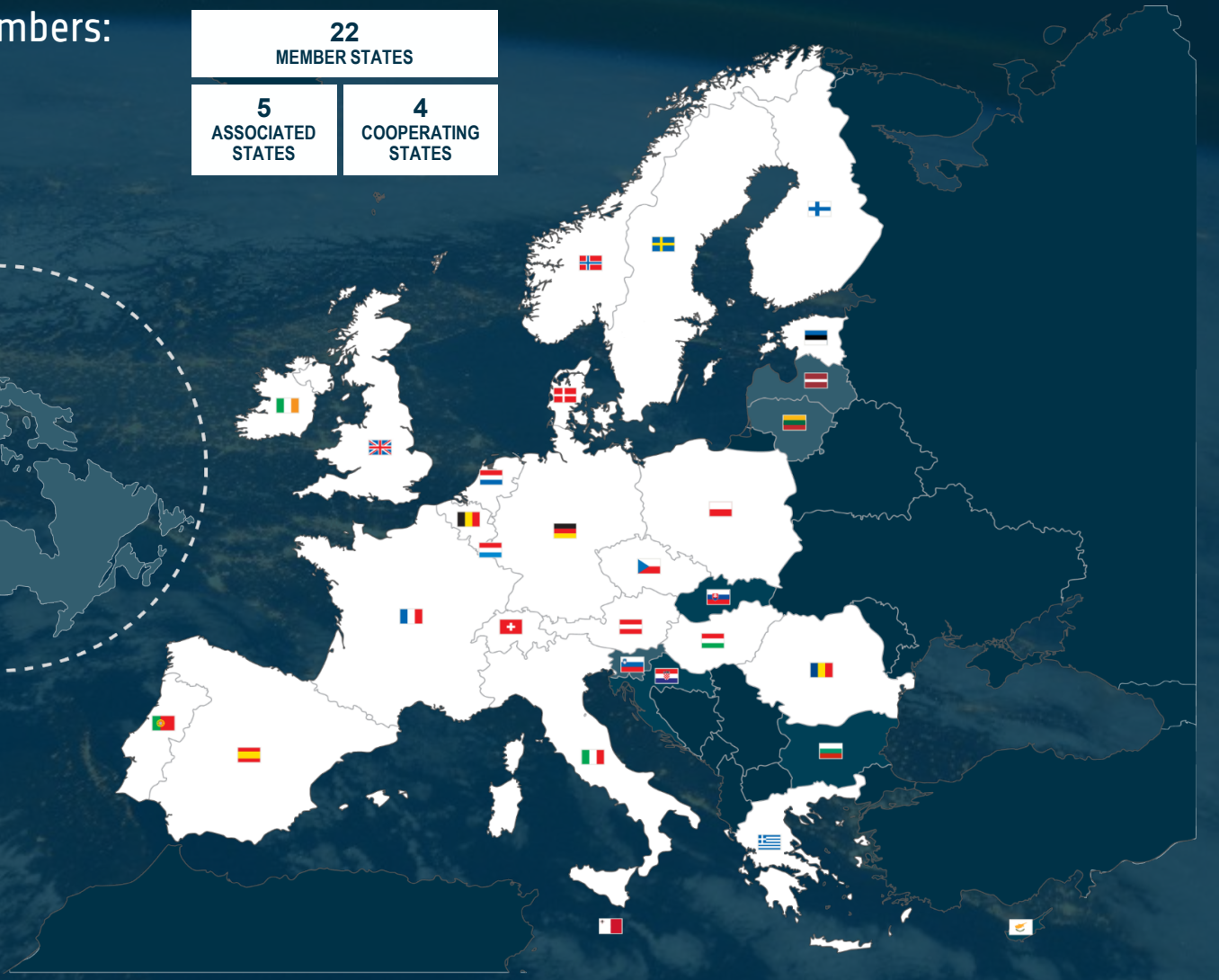
Goals:

1. Explore the Universe
2. Improve life on Earth

Pacific purposes

Members:

22 MEMBER STATES	
5 ASSOCIATED STATES	4 COOPERATING STATES



Activities:

- Earth Observation
- Human & Robotic Exploration
- Space Transportation
- Navigation (Galileo)
- Telecom & Integrated Apps
- Science
- Operations
- **Space Technology, Engineering & Quality**

Outline

1. Who?
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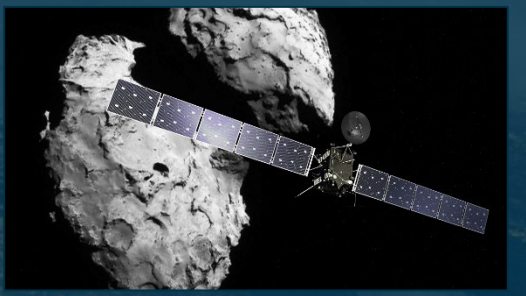
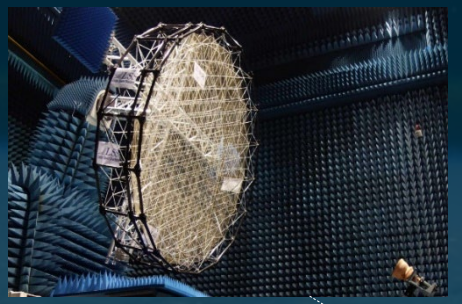


1.2 Who? – ESA ESTEC

- ESA's Space Research and Technology Centre
- Located in Noordwijk, The Netherlands, it provides:
  - ESA missions are developed and managed
  - ESA's test centre for systems and S/Cs:
    - Labs
    - Anechoic chambers
    - Biggest vacuum chamber in Europe
    - Loudest sound facility in EU
    - Vibration platforms
    - ..
  - Cooperation with space agencies all over
  - Support for European space industry and universities, research institutes and national agencies from ESA Member States



ECSAT (Harwell)

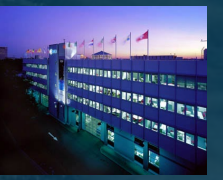
ESTEC (Noordwijk)

EAC (Cologne)

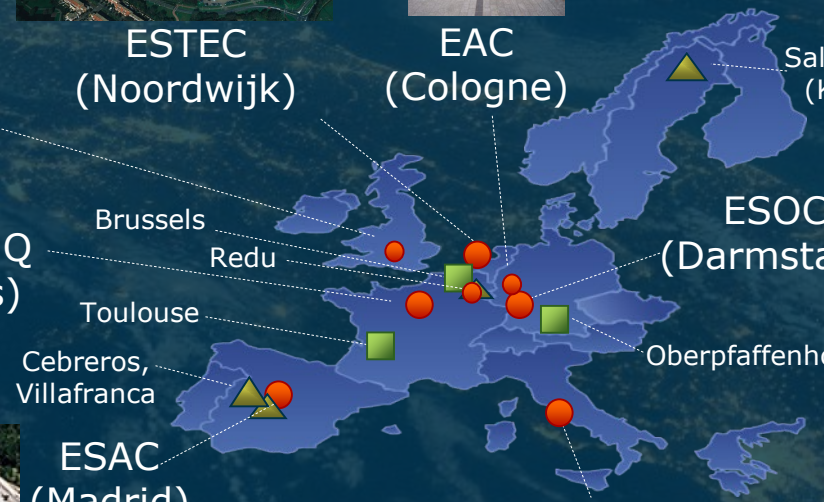
ESA HQ (Paris)

ESAC (Madrid)

ESRIN (Rome)



ESOC (Darmstadt)



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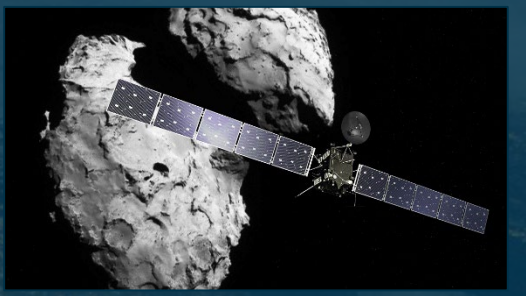
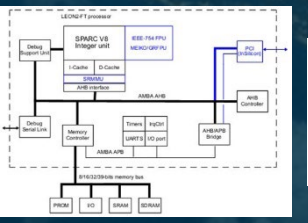


1.3 Who? – ESA ESTEC-EDM

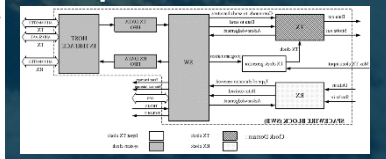
- **TEC** - Directorate of Technology, Engineering and Quality
  - **E** - Electrical Department
    - **D** - Data Systems and uElectronics Division
      - **M** - uElectronics Section
- TEC-EDM Responsibilities:
  - Support to Missions (MSR, Metop, Galileo…)
    - ASICs & FPGAs (SRR, PDR, CDR, DDR, AR/QR)
  - Support to developments needed by the EU Space ecosystem in the future (R+D):
    - ICs: digital/analog/mixed-signal
    - IP Cores
    - EDA Tools
  - In house activities:
    - Standards
    - Conferences/Workshop organization
    - Laboratory for independent validation of the new technologies

CAES PIONEERING ADVANCED ELECTRONICS
SIEMENS
AMD XILINX
MICROCHIP
MATLAB
SYNOPSYS
cadence
NanoXplore

Leon2-FT



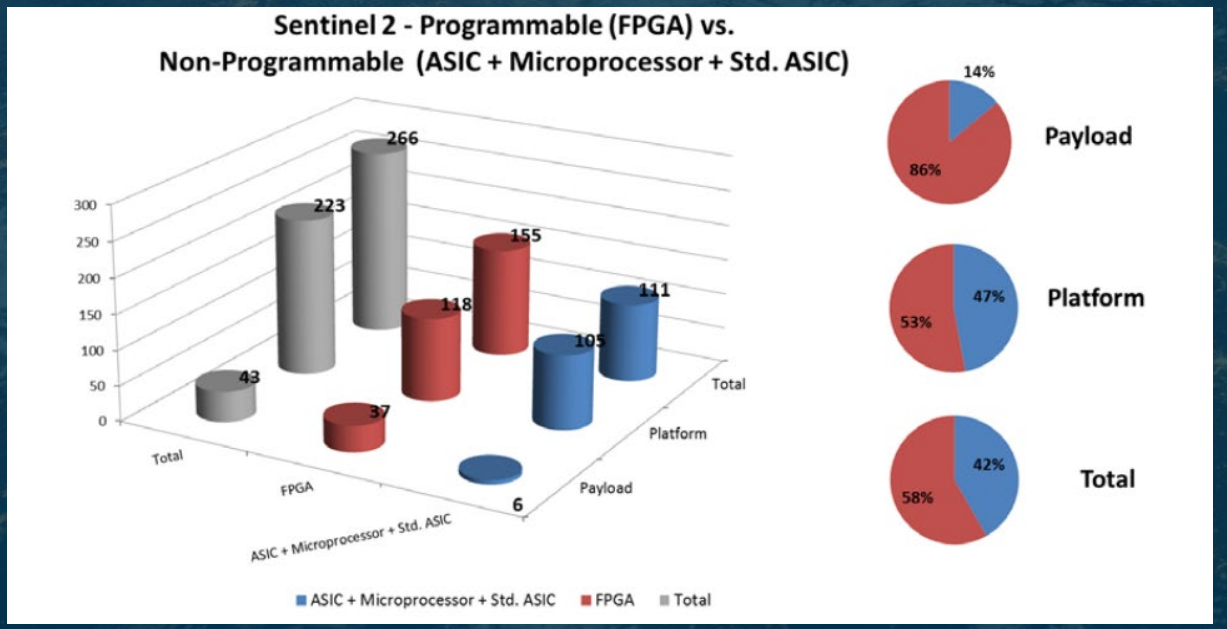
SpW Codec



1.3 Who? – ESA ESTEC-EDM

- How important are uElectronics in S/C?

Sentinel 2 integrated circuits survey (2013) → total ICs= 266



Trends and patterns of ASIC and FPGA use in European space missions. Agustin Fernández León (ESA)

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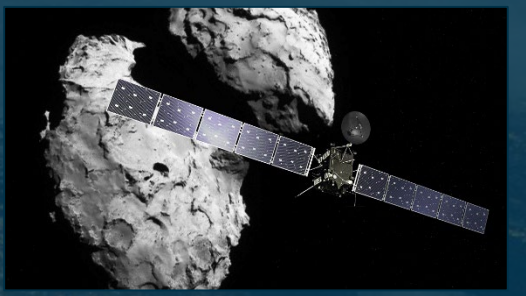
2. R+D activities
    1. Rad-Hard European FPGAs: a new player in the market



2.1 R+D activities - Rad-Hard EU FPGAs: a new player in the market

Main Goal: Provide to the Space Industry a high-capacity, well performant rad-hardened reprogrammable EU FPGAs

Requirements:

- Competitive FPGA capacity, performance and radiation hardness to be used in a wide range of space equipment across all ESA missions: Science, Exploration, Earth Observation, Telecom, Navigation, Space Transportation and Human Spaceflight.
- Unlimited re-programmability: versatile and adaptive, as FPGAs are.
- Extend and keep the European competence on FPGAs and capability to specify and develop state of the art FPGAs for space.

BRAVE: **B**ig **R**e-programmable **A**rray for **V**ersatile **E**nvironments

Consortium:

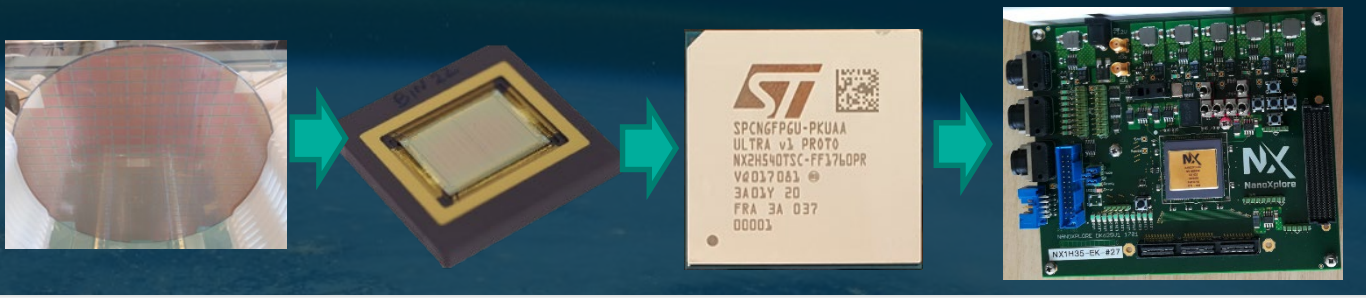
NanoXplore	STMicroelectronics	AIRBUS / ThalesAlenia Space	European Commission / esa / cnes
Development (fabless) CAD FPGA tools Sales Customer Support	Foundry Packaging Test Eval & Qual	Reqs. definition Review milestones Beta users NG-ULTRA: dev. team	Technical review & support Economical support

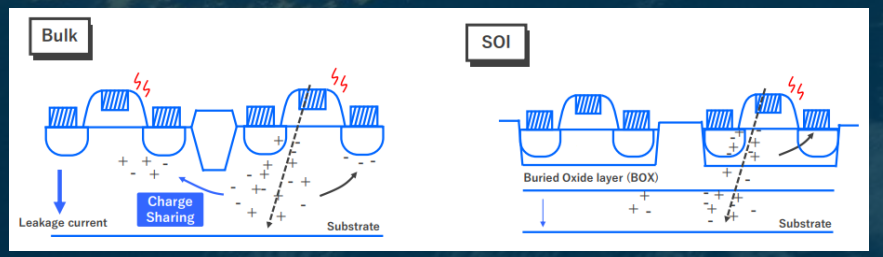
2.1 R+D activities - Rad-Hard EU FPGAs: a new player in the market

Roadmap

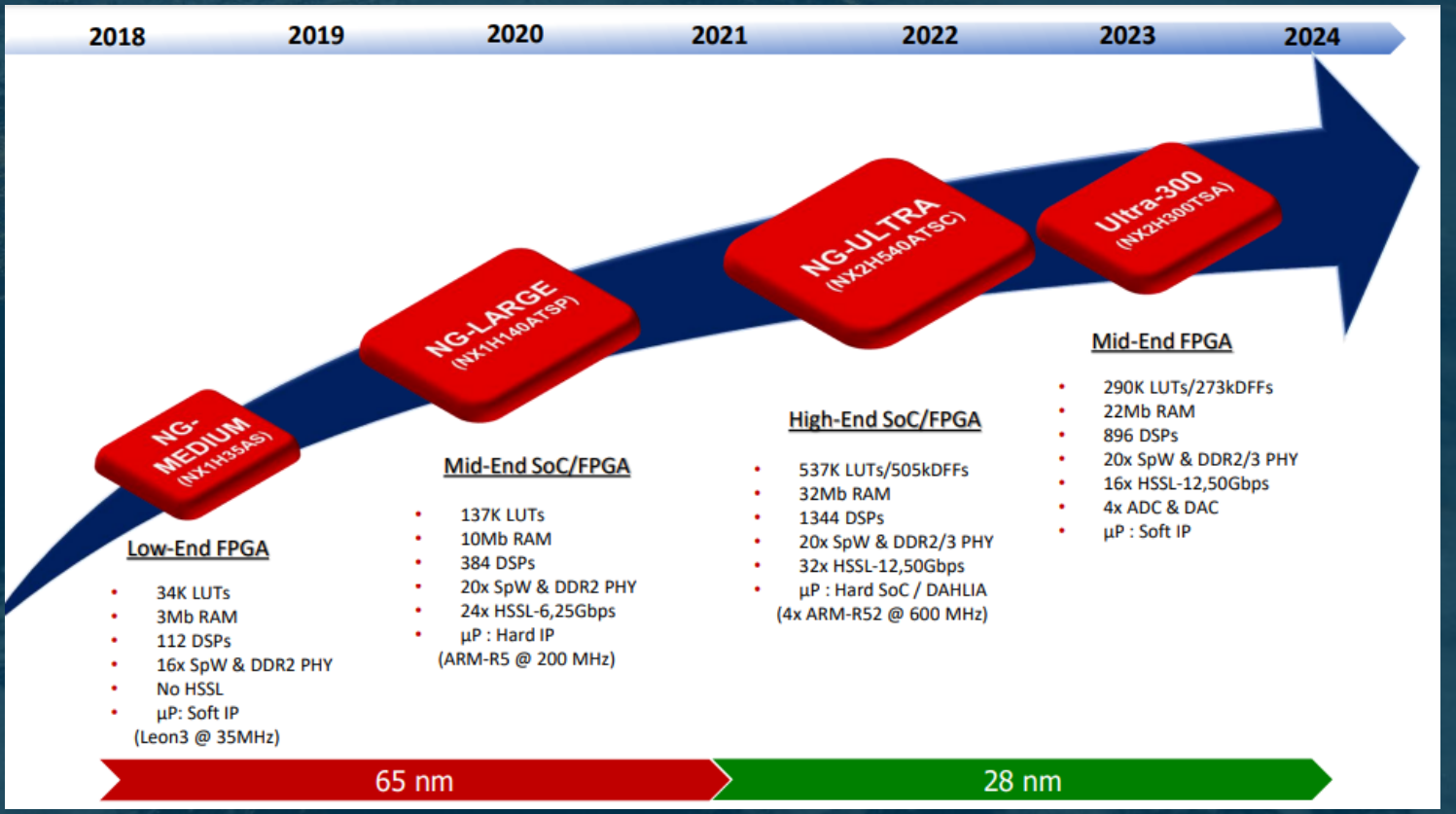
- Rad-hard FPGAs (to be) qualified for space applications
- SRAM based
- From FPGA+ to SoC FPGA
- From 65nm Bulk CMOS to 28nm FD-SOI by STM
- RHBP FD-SOI improves radiation performance
- Lower power consumption (< leakage, < static)
- Designed and manufactured in EU

- Next generation on 7nm? State of the art!





Keita Sakamoto (Jaxa)

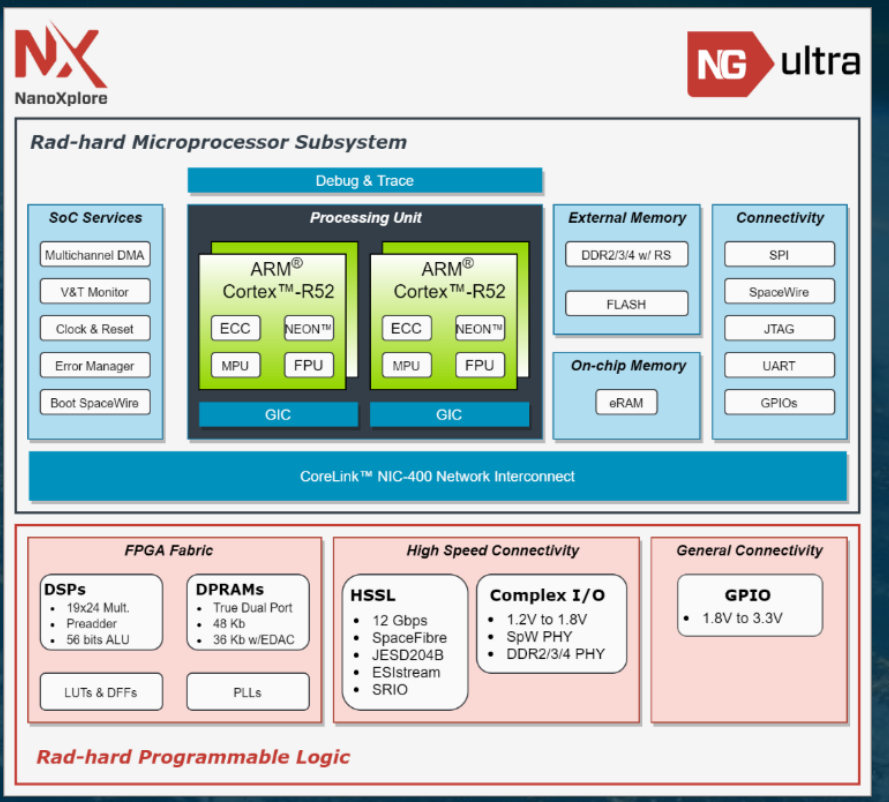


FPGA Portfolio & Roadmap (NanoXplore)

2.1 R+D activities - Rad-Hard EU FPGAs: a new player in the market

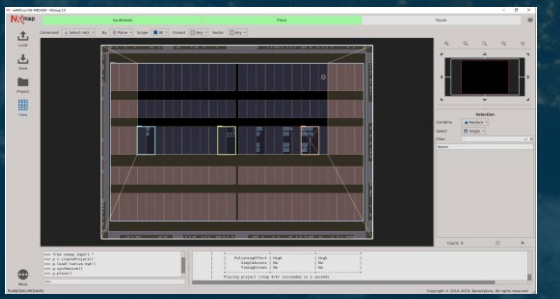
NG-Ultra - SoC FPGA in a single chip:

- **RHBD**: EDAC for RAM + DICE (6T->12T) cells for CMem/DFFs + Scrubber for CMem
  → no need for mitigation techs by users
- Processing system: Quad-Core ARM R52 @ 600 MHz + FPU
- Memories:
  - Boot eROM + 2 MBytes eRAM w/ ECC
  - Interface to volatile (Hard IP) Mems: DDR2/DDR3/DDR4
  - Interface to non-volatile (Hard IP) Mems: Flash
  - 16 channels DMA to support memory transfers
- Interconnect: AXI-based network
- Programmable logic: 500 KLUTs
- HSSL (Hard IP)
- Security features (e.g. bitstream encryption)
- Radiation performance:
  - SEU/SEL/SEFI immune up to 68MeV/g/cm3
  - TID: 50 krads (Si)



EDA tools:

- Nx-Map/Nx-Python: Synthesis, P&R (Mentor Precision for NG-Ultra)
- Nx-Core for IP cores management and import
- Nx-Scope as ILA
- Nx-SDK for SW development + ARM ecosystem for debug and trace

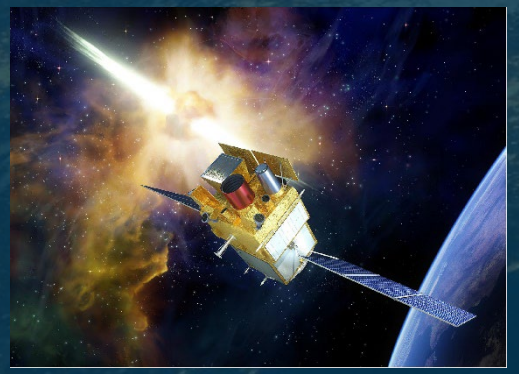


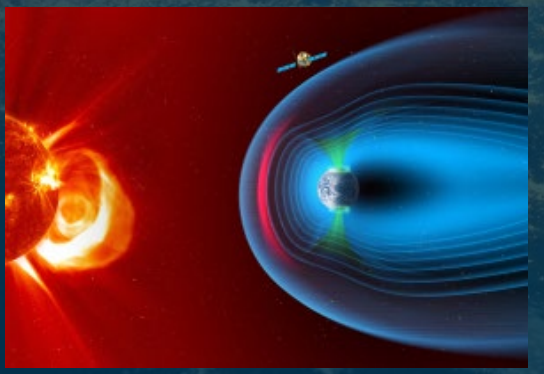
nxmap

2.1 R+D activities - Rad-Hard EU FPGAs: a new player in the market

To be launched soon:

- SVOM (Space Variable Objects Monitor)
- SMILE (Solar wind Magnetosphere Ionosphere Link Explorer)
- GOMX-5 A & B





References:

- Systematic Evaluation of the European NG-LARGE FPGA & EDA Tools for On-Board Processing. 2nd OBDP: European Workshop on On-Board Data Processing – June 2021
- NanoXplore - Linux goes to space in Ultra. 16th ADCSS: ESA Workshop on Avionics, Data, Control and Software Systems – October 2022
- ADS - NG-Ultra, the European rad-hard multicore ARM system-on-chip + FPGA suitable for future space applications. 16th ADCSS: ESA Workshop on Avionics, Data, Control and Software Systems – October 2022
- QUEENS-FPGA: Quality Evaluation of European New SW for the BRAVE FPGA. 4th SEFUW: SpacE FPGA Users Workshop, 4th Edition

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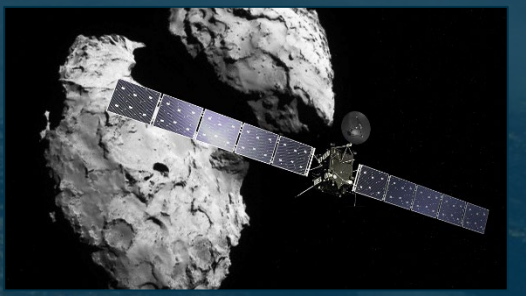
    1. Rad-Hard European FPGAs: a new player in the market.
    2. Upcoming IPs



2.2 R+D activities: upcoming IPs

An **IP** (Intellectual Property) Core is an "off-the-shelf" building block for creating larger digital designs, delivered in the form of source code (computer files of hardware description language) and associated documentation.

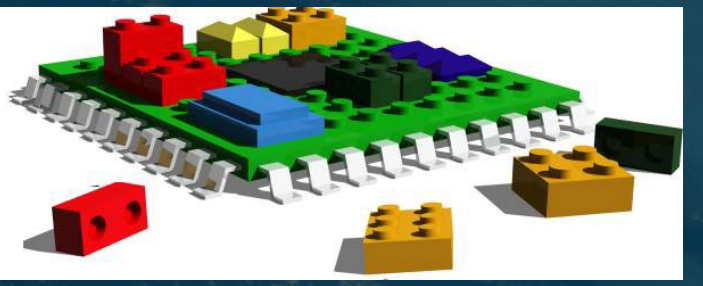
IP Cores are designed and extensively verified for re-use as building blocks of integrated circuits such as ASICs or FPGAs.

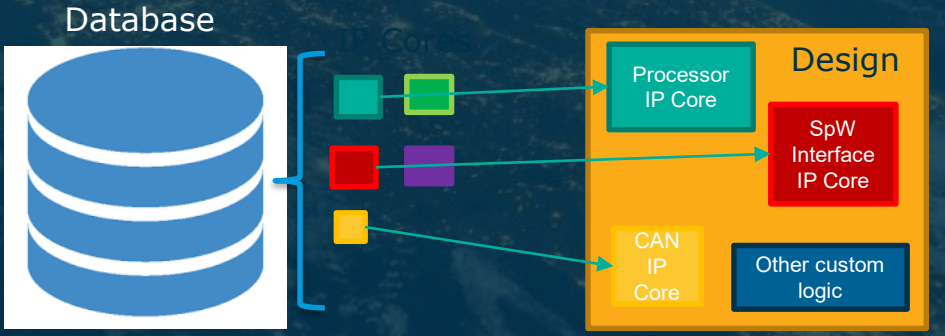
Upsides:

- Guarantees compliance with standardised functions or communication protocols.
- Verification of the building block is not needed (unless modified).
- Reduces overall risks.
- Saves time and costs needed to develop the IP function.

Downsides:

- Knowledge not acquired.
- 3rd party dependent.
- Economic cost?





ESA/ESTEC maintains and distributes a small catalogue of IP Cores for space applications. They can be licensed for research and/or commercial use, under specific conditions to companies/consortiums based in ESA members and participants states.

2.2 R+D activities: upcoming IPs

SHyLoC 2.0: Multi/Hyperspectral Lossless Compression

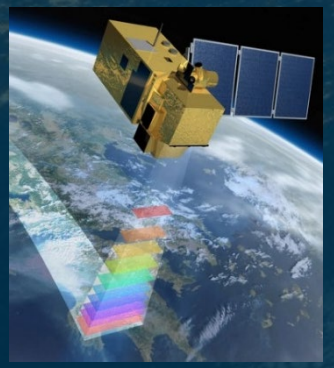
Data is needed to achieve the goal of missions, but not always possible to download it directly to ground:

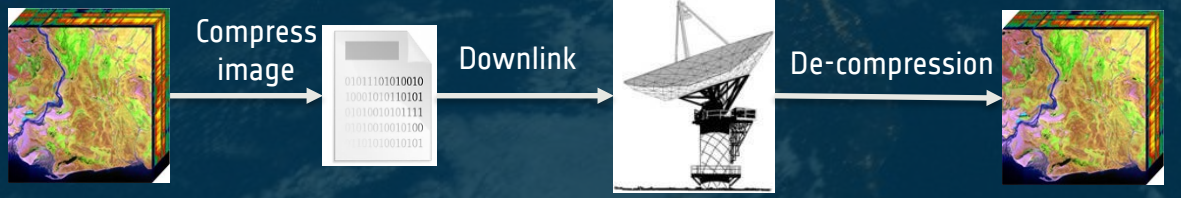
- S/C is out of sight of ground station
- Data acquisition rate ≠ downlink rate

ADS

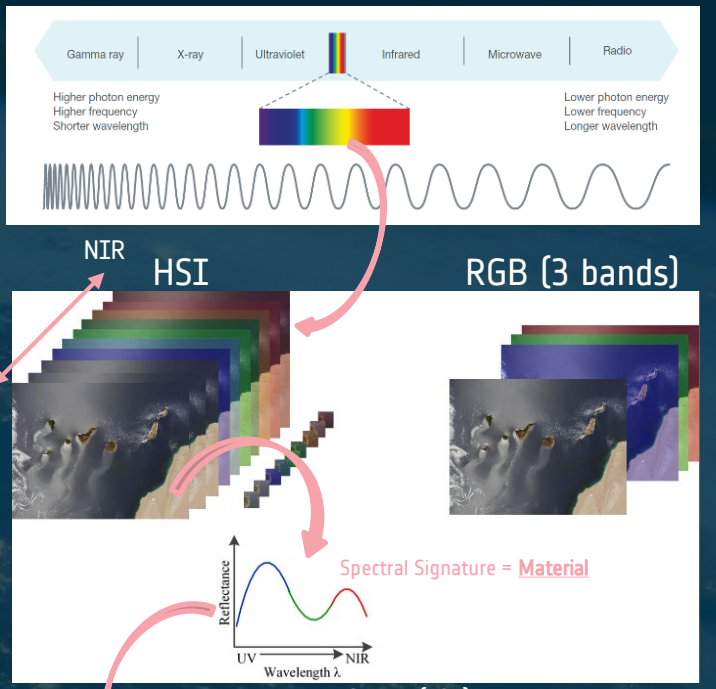
To apply **compression** on-board the S/C: payload data processors shall be powerful and efficient → Max. reduction & min resources!

Consortium:


EO mission



Dr. Lucana Santos (ESA)



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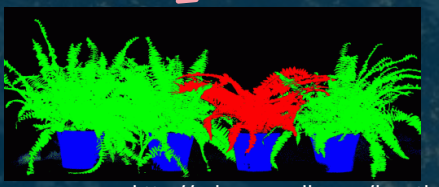
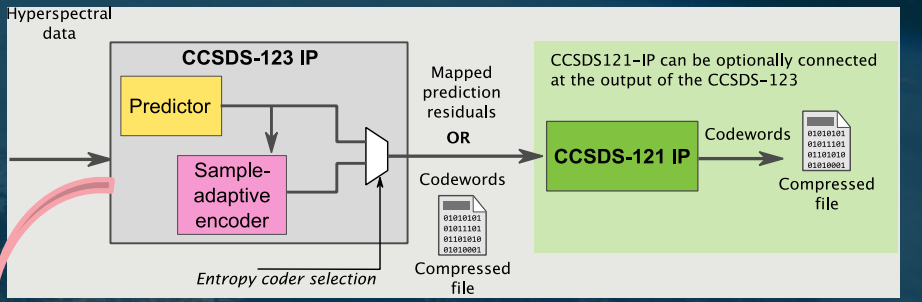


http://sciencenordic.com/lengthy-can-do-list-colour-camera

2.2 R+D activities: upcoming IPs

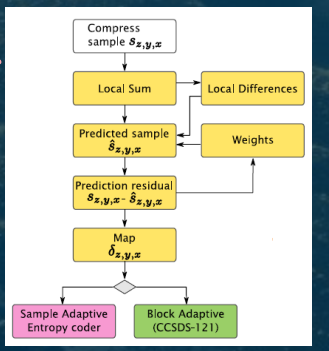
SHyLoC 2.0: Multi/Hyperspectral Lossless Compression

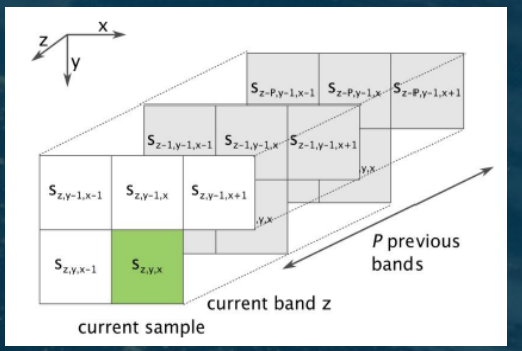
Lossless compression reduces the data volume without compromising the data integrity (the image can be fully recovered after decompression).



CCSDS
(Consultative Committee for Space Data Systems)

x2 IP Cores part of ESA portfolio





CCSDS 123.0-B-1
Lossless Multi / Hyperspectral Image Compression

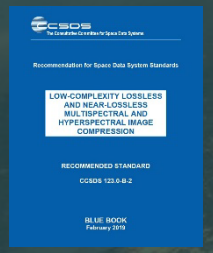
CCSDS 121.0-B-2
Lossless Data Compression

Compatible technologies:
- -RTAX (OTP)
- -Virtex5 QR
- -ProASIC3E/RTG4
- -NG-Medium/NG-Large
- -ASIC DARE 180nm (standard cell lib)

Performance:
- -Up to 113.7 Msamples/s for 16b input in Virtex5QR

2.2 R+D activities: upcoming IPs

Lossless and Near-Lossless Multi/Hyperspectral Image Compression



CCSDS 123.0-B-2 Low-Complexity Lossless and Near-Lossless Multispectral and Hyperspectral Image Compression

-Released in 2019
-Near lossless more compression ratio than lossless, by quantization
-Image quality control ensured, mandatory for space applications
-Configurability vs. resources use

Efficient Video Compression for Space

H264 – Advanced Video Coding

-Not a new standard (1st release in 2004)
-It has become a need also in space applications
-Full compliance with a commercial standard video codec
-RGB and monochrome
-Aspect ratios: optimized for 4:3 and 16:9
-Resolutions: 320x240, HD(1280x720), UHD(3840x2160)
-Frame rates: 120fps low, 30fps HD & 10fps UHD
-SW independent

Common:

-AHB/AXI for raw input and compressed output streams
-SEE mitigation techniques: deadlock free FSMs, soft TMR and ECC for memories at least
-Technology independent RTL (no macro instantiation)
-Approach: trade off with HLS model -> design at RTL -> verification -> implementation -> validation
-Technologies addressed: Xilinx KU060, Microchip PolarFire/RTG4, NX Brave

2.2 R+D activities: upcoming IPs

References:

- CCSDS: Consultative Committee for Space Data Systems
- Lossless Multispectral & Hyperspectral Image Compression. Recommendation for Space Data System Standards, CCSDS 123.0-B-1. Blue Book. Issue 1. Washington, D.C.: CCSDS, May 2012.
- Lossless Data Compression. Recommendation for Space Data System Standards, CCSDS 121.0-B-2. Blue Book. Issue 2. Washington, D.C.: CCSDS, April 2012.
- Low-Complexity Lossless and Near-Lossless Multispectral and Hyperspectral Image Compression, Recommendation for Space Data System Standards , Blue Book, Issue 2, CCSDS 123.0-B2, 2019
- Advanced Video Coding for Generic Audiovisual Services. ITU-T H.264. Geneva: ITU, 2012.
- 8th OBPDC: International Workshop on On-Board Payload Data Compression – September 2022 – Athens
- L. Santos, A. Gómez and R. Sarmiento, "Implementation of CCSDS Standards for Lossless Multispectral and Hyperspectral Satellite Image Compression," in IEEE Transactions on Aerospace and Electronic Systems, vol. 56, no. 2, pp. 1120-1138, April 2020
- Y. Barrios, A. J. Sánchez, L. Santos and R. Sarmiento, "SHyLoC 2.0: A Versatile Hardware Solution for On-Board Data and Hyperspectral Image Compression on Future Space Missions," in IEEE Access, vol. 8, pp. 54269-54287, 2020, doi: 10.1109/ACCESS.2020.2980767

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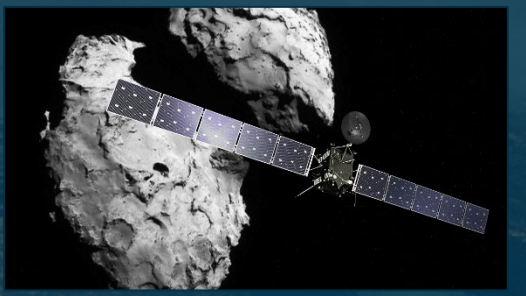
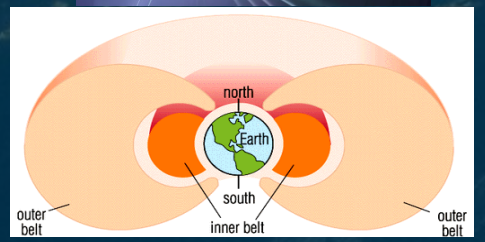


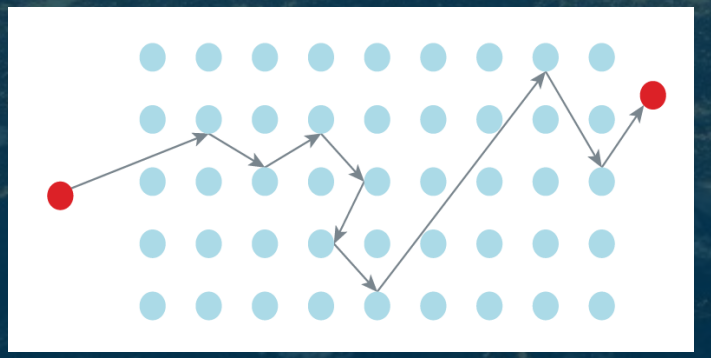
2.3 R+D activities: FPGAs on-board reliable reconfiguration

R^3 FPGAs = Reliable Reconfiguration under Radiation of FPGAs

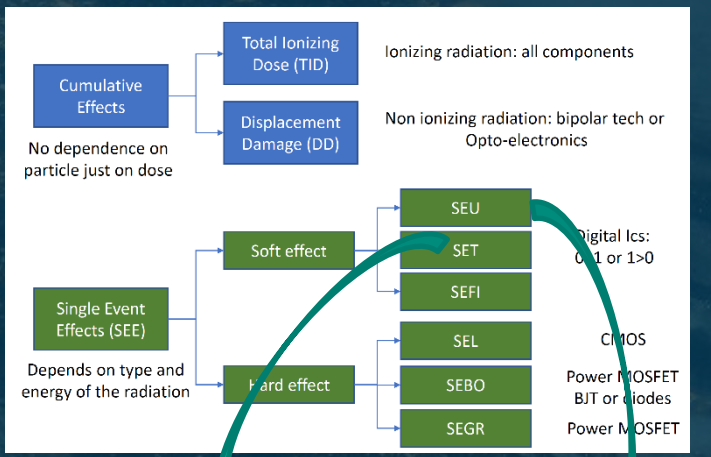
Study reliable total/partial reconfigurable architectures on technologies from x3 main vendors: Xilinx, Microchip & NanoXplore

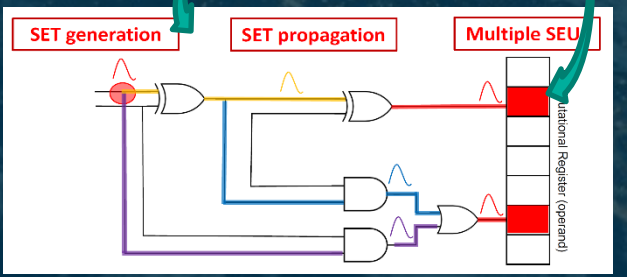
Why reliability is that important: Space is a harsh environment → **Radiation!**





Radiation Handbook for Electronics – Texas Instruments





Consortium:

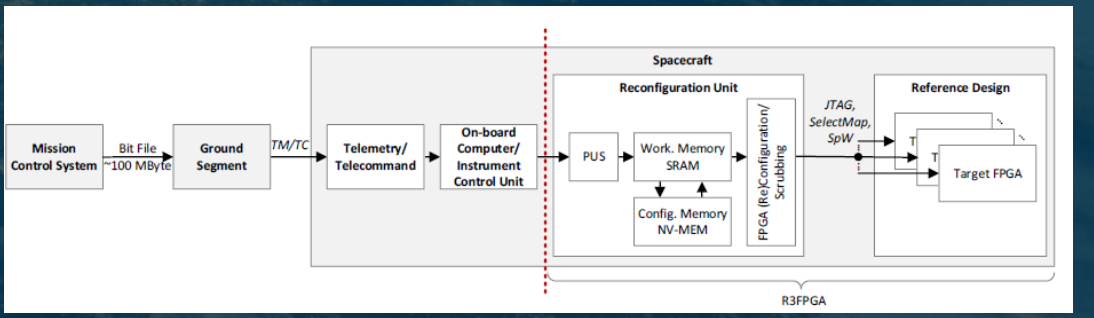
2.3 R+D activities: FPGAs on-board reliable reconfiguration

Solutions already flying in Solar Orbiter, Mars Perseverance Rover...
but targeting a particular device and setup, normally Virtex 4QV and Virtex 5QV

R^3 FPGAs = Reliable Reconfiguration under Radiation of FPGAs

- Use cases:
  - Multiple behaviours in a single device
  - Correct faulty in-flight designs
  - Update/extend functionality
- Bitstreams preloaded before flight, or updated during flight

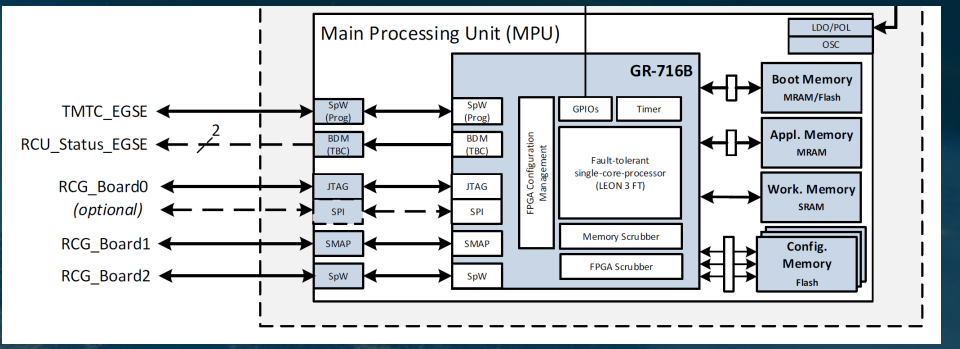
- Targeted technologies:
  - Xilinx XQRKU060 (SRAM)
  - Microchip RT PolarFire RTPF500 (Flash)
    Limited re-programmability 500/2000 config. cycles
  - NX NG-Medium NX1H35AS (RHBD SRAM)
    smaller device, though representative



R3FPGA envisaged use in S/Cs

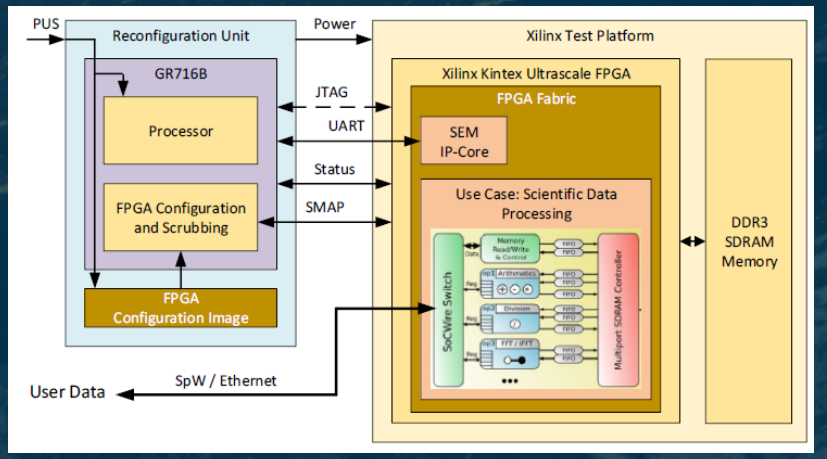
2.3 R+D activities: FPGAs on-board reliable reconfiguration

- Full and partial in-flight reconfiguration targeted
- Reliability, availability, power consumption and data rates analysed.
- External memory where the different configuration bitstreams are allocated.
- Rad Hard controller to manage that NV memory (GR716B selected)
- Golden reference bitstream accessible if non-recoverable faults during reconfig.
- CMem needs scrubbing in SRAM based FPGAs to avoid their accumulation
- Independent channels: one for config and scrubbing vs. one for comms
- Reconfiguration triggered by:
  - -External signal to the FPGA or TC from ground (change version/uploaded one)
  - -By a timer due to operational needs (pool of versions in a mem)



Reconfiguration Unit: based in MCU GR716B

Xilinx Ultrascale KU060

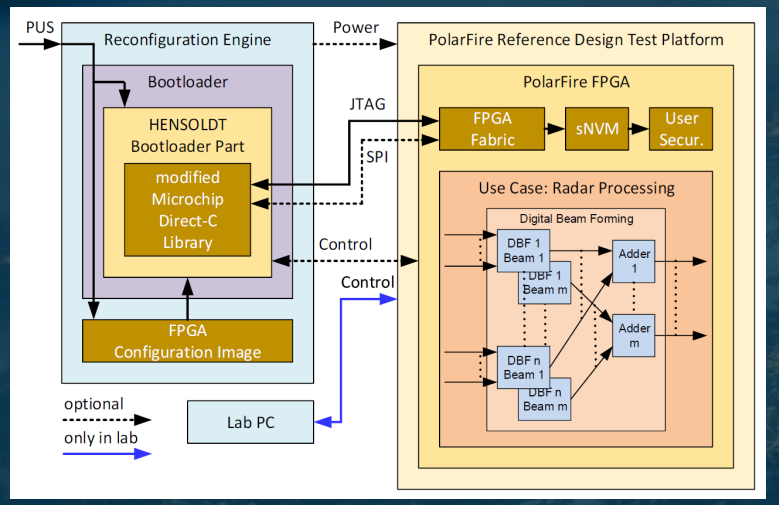


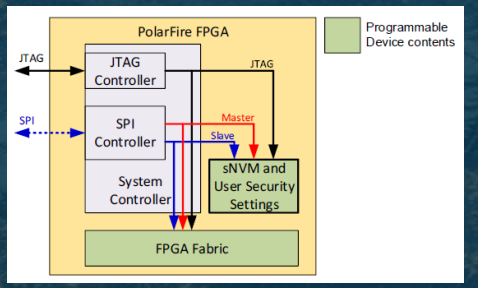
Xilinx KU060 approach with external reconfiguration engine:

- Reconfiguration engine with ext. scrubber
- Partial reconfiguration supported
- Slave SelectMap (8b parallel)
- 80MHz for SelectMap (1.2secs)
- 1MHz for JTAG as backup (3.5min)
- SEFI detected and corrected
- Voltage and current monitors

2.3 R+D activities: FPGAs on-board reliable reconfiguration

Microchip RT Polarfire 500

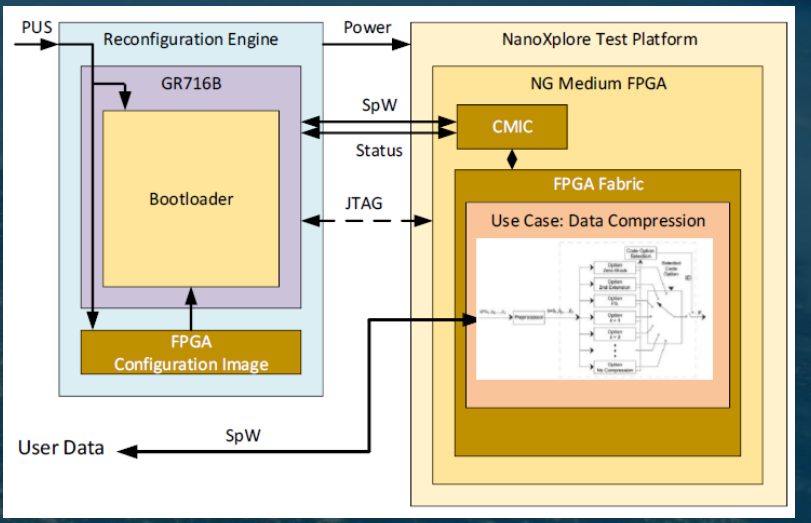




Microchip RT PolarFire 500 approach with external reconfiguration engine

- Dynamic partial reconfiguration dismissed, not supported. Flash based and limited cycles
- Reconfiguration engine with External scrubber
- System Controller needed, but not radiation hardened!
- 4MHz for JTAG (120secs)
- SPI Slave configuration as backup @ 80MHz
- SPI Direct-C library provided for the external processor
- SEFI detected and corrected

NX Brave Medium



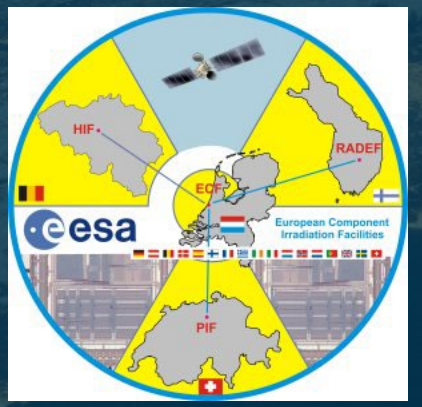
NX Brave Med approach with external reconfiguration engine

- Reconfiguration engine without external scrubber
- Dynamic partial reconfiguration dismissed, future feature
- Internal scrubber (CMIC = Cofig. Memory Integrity Check hard core)
- 50MHz for SpaceWire (1sec)
- 1MHz for JTAG as backup (1.5mins)
- SEFI detected and corrected
- Main Power supply supervised by the reconfiguration engine

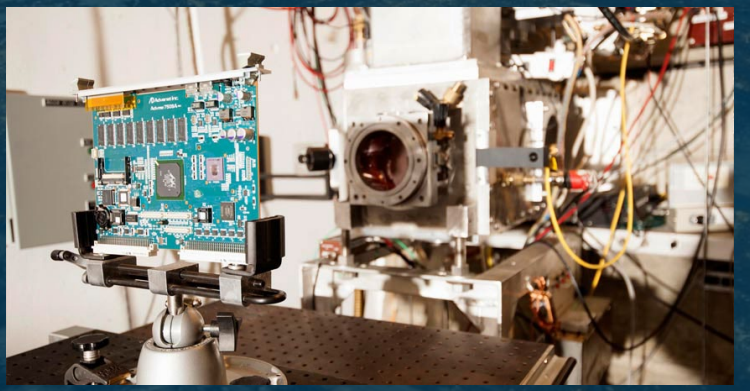
2.3 R+D activities: FPGAs on-board reliable reconfiguration

Radiation campaign:

- Validate the design under a representative emulated harsh environment → radiation beam generated in a particles accelerator
- Normally, heavy ions and protons at least, and at different energies



European Component Irradiation Facilities



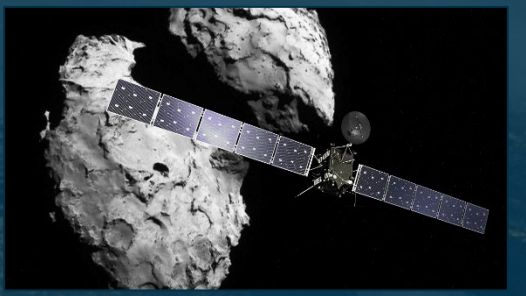
FPGA under radiation testing

References:

- Microchip Polarfire, Xilinx UltraScale, NanoXplore Brave and Gaisler GR716A online documentation
- The Mars 2020 Engineering Cameras and Microphone on the Perseverance Rover: A Next-Generation Imaging System for Mars Exploration. Space Sci Rev (2020) 216:137

Outline

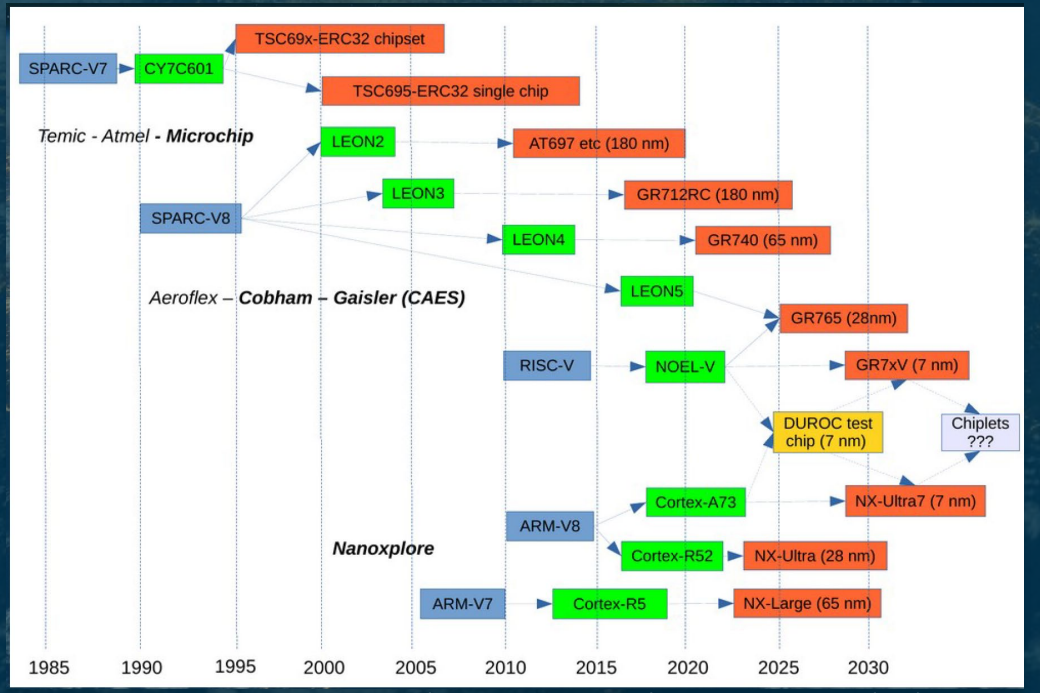
1. Who?
    1. ESA
    2. ESTEC
    3. TEC-EDM
2. R+D activities
    1. Rad-Hard European FPGAs: a new player in the market
    2. Upcoming IPs
    3. On-board reliable reconfiguration
    4. RISC-V activities



2.4 R+D activities: RISC-V activities

General roadmap in EU space ecosystem:

- 30 years SPARC
- 25 years of LEON in Space
- ARM was getting its niche from 2005, and it might have gotten a piece of the cake for another 20yrs…
- …but RISC-V was born in 2011 @ Berkeley and ever since, it's been gaining momentum all around in the last +3 years



Space Microprocessors in EU (not an ESA roadmap) - Roland Weigand (ESA)

2.3 R+D activities: RISC-V activities

Upsides:

- License independent ISA (open source as SPARC) & not single-vendor proprietary as ARM
- Geopolitically independent: RISC-V organisation (riscv.org) based in Switzerland
- Strong academic and industrial support (widespread)
- Growing SW ecosystem in the market (toolsets, libraries, engines..)
- Low silicon floor requirements → better density and scalability
- Modularity: versatile base 32b/64b/128b ISA + several standard extensions to cover from MCU/MPU to HP/AI (H=Hypervisor, V=Vector or P=packed SIMD)
- Room for custom extensions

Downsides:

- Context change cost
- Not yet mature enough for some applications

-Seems to be the obvious choice for Space in the coming years!

-We need to support the trend to standardize RISC-V use all over the different computing products (MCU, MPU, SoC, FPGA SoCs, COTS, HPC...)

-Cobham Gaisler and Microchip have already transitioned towards RISC-V

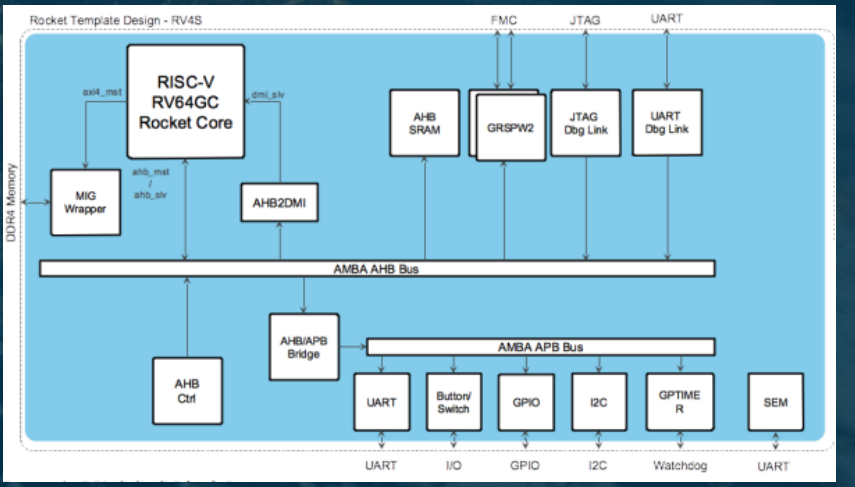
ISA base and extensions

Name	Description	Version	Status[b]	Instruction count
Base				
RVWMO	Weak Memory Ordering	2.0	Ratified	
RV32I	Base Integer Instruction Set, 32-bit	2.1	Ratified	40
RV32E	Base Integer Instruction Set (embedded), 32-bit, 16 registers	1.9	Open	40
RV64I	Base Integer Instruction Set, 64-bit	2.1	Ratified	15
RV128I	Base Integer Instruction Set, 128-bit	1.7	Open	15
Extension				
M	Standard Extension for Integer Multiplication and Division	2.0	Ratified	8 (RV32) 13 (RV64)
A	Standard Extension for Atomic Instructions	2.1	Ratified	11 (RV32) 22 (RV64)
F	Standard Extension for Single-Precision Floating-Point	2.2	Ratified	26 (RV32) 30 (RV64)
D	Standard Extension for Double-Precision Floating-Point	2.2	Ratified	26 (RV32) 32 (RV64)
Zicsr	Control and Status Register (CSR)	2.0	Ratified	6
Zifencei	Instruction-Fetch Fence	2.0	Ratified	1
G	Shorthand for the IMAFDZicsr_Zifencei base and extensions	—	—	
Q	Standard Extension for Quad-Precision Floating-Point	2.2	Ratified	28 (RV32) 32 (RV64)
L	Standard Extension for Decimal Floating-Point	0.0	Open	
C	Standard Extension for Compressed Instructions	2.0	Ratified	40
B	Standard Extension for Bit Manipulation	1.0	Ratified	43[28]
J	Standard Extension for Dynamically Translated Languages	0.0	Open	
T	Standard Extension for Transactional Memory	0.0	Open	
P	Standard Extension for Packed-SIMD Instructions	0.9.10	Open	
V	Standard Extension for Vector Operations	1.0	Frozen	187[29]
K	Standard Extension for Scalar Cryptography	1.0.1	Ratified	49
N	Standard Extension for User-Level Interrupts	1.1	Open	3
H	Standard Extension for Hypervisor	1.0	Ratified	15
S	Standard Extension for Supervisor-level Instructions	1.12	Ratified	4
Zam	Misaligned Atomics	0.1	Open	
Ztso	Total Store Ordering	0.1	Frozen	

2.4 R+D activities: RISC-V activities

RV4S – RISC-V for Space

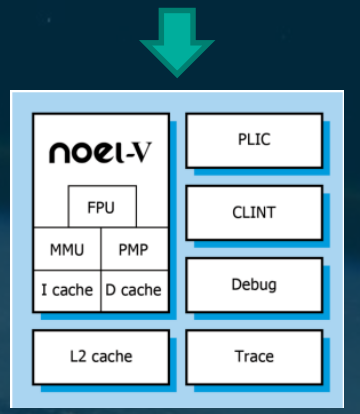
- Evaluation of existing RISC-V IP cores (Berkeley Rocket, LowRISC, Boom, SHAKTI…) and suitability for space systems
- M, F, D, A extensions necessary as a min for space applications
- Rocket finally selected! Configuration: 12KB L1 I-D cache, double precision FPU, AXI4 interface to memory
- Implemented in a Xilinx Ultrascale FPGA
- SEU mitigation techniques included: SECDED for memories and distributed TMR mainly + single event fault injection verification
- Completed in 2019
- More info: RV4S



2.4 R+D activities: RISC-V activities

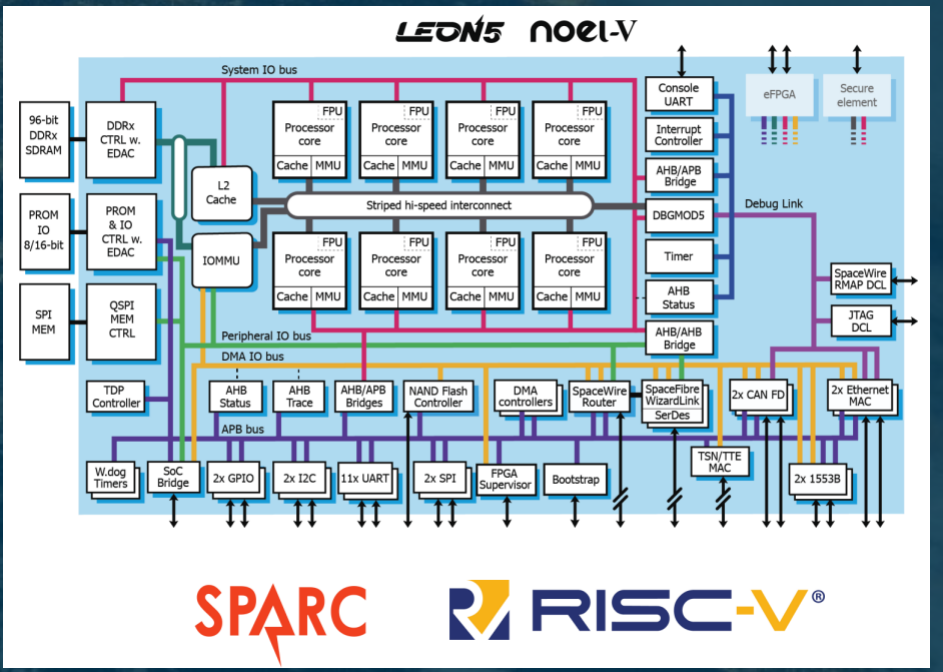
NOEL-V IP

- Cobham Gaisler transition to RISC-V: NOEL-V → GR765 → GR7xV
- Fully available as a free open source IP from GRLIB, for FPGAs/ASICs
- 32b/64b + single/double precision + compressed + HW hypervisor
- Multi core support
- Fault tolerant approach
- Used for the development of GR765



GR765 Multi-Core SoC

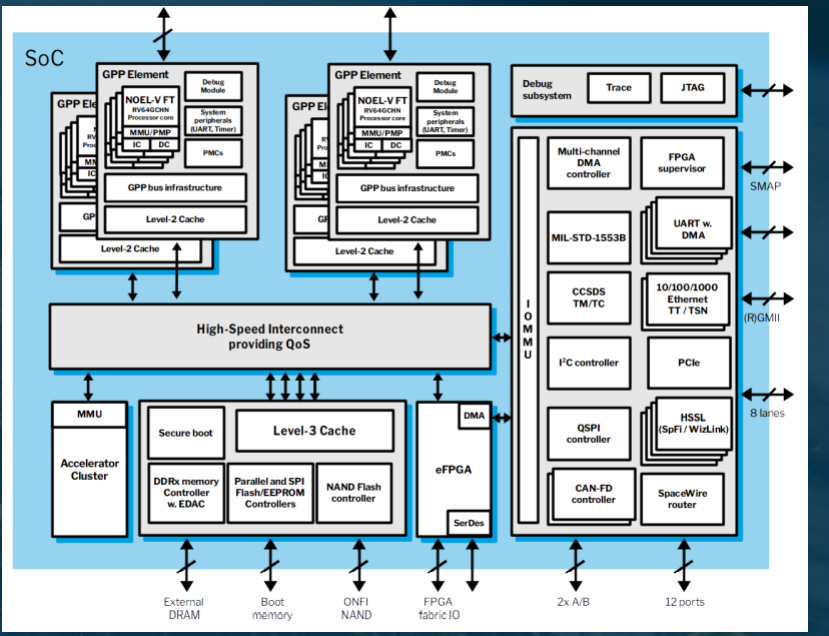
- Octa-Core in STM FD-SOI 28nm @ 1GHz with 2MB L2 cache
- From LEON5FT only to dual mode (32b LEON5FT or 32b/64b NOEL-V FT)
- SPARC still addressed as a transition, more mature and know-how
- Prototypes expected in mid-2024, FM 2025, QML 2026
- Mems: DDR3, NAND Flash, (Q)SPI mem controllers.. protected with ECC
- Itfs: x4 SpF, SpW router, x2 10/100/1000Mbps Eth, x2 TTE, x2 1553..
- FPGA supervisor + eFPGA (30k LUT envisaged) for HW accelerators



2.4 R+D activities: RISC-V activities

GR7xV SoC

- Hexadeca-core with x4 GPP islands in TSMC 7nm @ xMHz
- 64b NOEL-V FT
- L2 cache for each island
- L3 cache shared among all x16 cores through high speed interconnect
- eFPGA (30k LUT envisaged) for HW accelerators
- Architectural Design started Q3/2021, HW > 2025
- Mems: DDRx, NAND Flash.. protected with ECC
- Itfs: SpW router, SpF, 10/100/1000Mbps Eth/TTE/TSN, 1553…



References:

- **RISC-V for Space** - RV4S
- Cobham Gaisler's Noel-V IP Core
- Cobham Gaisler - GR740, GR765 and GR7xV: SPARC V8 and RISC-V for On-Board Computing - ADCSS'22: 16th ADCSS: ESA Workshop on Avionics, Data, Control and Software Systems – October 2022
- Spin-in of RISC-V Processors in Space Embedded Systems - PhD Thesis – Stefano Di Mascio (TU Delft) – September 2022
- Upcoming event: RISC-V in Space Day + GR740 Day – 13th/14th of December 2022 in ESA/ESTEC (NL)

2.4 R+D activities: RISC-V activities

1st RISC-V processor in space on 2022! – TRISAT-R Mission

TRISAT-R

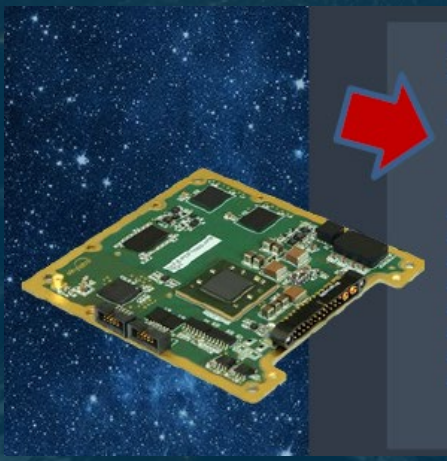
3U CubeSat mission targeting a MEO orbit and objective to perform a radiation analysis with four scientific payloads for radiation monitoring and IOD of several other technologies.

Mission and technologies

- IOD of a highly miniaturized nanoscale platform with fault tolerant features
- **IOD of first RISC-V processor (NOEL-V) in Space by CAES (Cobham Gaisler)**
- Provide mapping of ionizing radiation and radiation effects with on-board instruments:
  - RadMon from CERN
  - CHIMERA RHA from ESA
  - TID monitor from SkyLabs

- Prime University of Maribor, Slovenia
- Status **Phase D**

- Launch vehicle VEGA-C maiden flight in 2022
- Orbit MEO, 5865 km,
- Platform **NANOSky I (1st generation) avionics**
- Dimensions Nanosatellite, standard 3U form factor
- Communication UHF/VHF (GFSK)



NANOhpm-obc

High Performance Fault Tolerant RISC-V OBC

- Fault Tolerant **NOEL-V processor** @ 80 MHz
  - **RISC-V** 32-bit architecture
  - Single precision FPU / L2 cache
  - Implemented on Microchip Polarfire
- 256 MB DDR3 memory
- 4 Mbit NMV for TM storage (unlimited read/write endurance)
- Redundant 2Gb NAND Flash for mass storage
- Redundant CAN for TM/TC
- 2x High-speed LVDS or RS422/485 channels
- 8x GPIO (with multifunction support UART/SPI/TWI and OBT trigger)
- GNSS receiver on board (GPS / GLONASS / Galileo / BDS / QZSS)
- Compatible with the PC-104 form factor.

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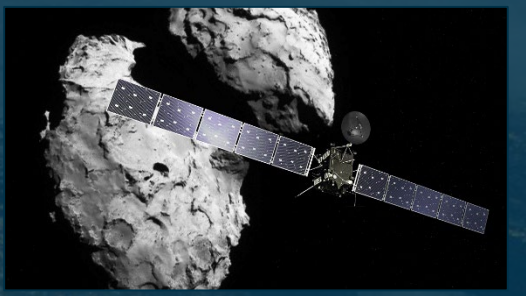
    4. RISC-V activities
    5. Others



2.5 R+D activities: Others

Radiation Hardened QNNs (Quantized Neural Networks)

G. Gambardella, N. J. Fraser, U. Zahid, G. Furano and M. Blott (Xilinx and ESA ESTEC), "Accelerated Radiation Test on Quantized Neural Networks trained with Fault Aware Training," 2022 IEEE Aerospace Conference (AERO), 2022, pp. 1-7, doi: 10.1109/AERO53065.2022.9843614

AI for FDIR (Failure Detection, Isolation and Recovery)

G. Furano, A. Tavoularis and M. Rovatti, "AI in space: applications examples and challenges," 2020 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), 2020, pp. 1-6, doi: 10.1109/DFT50435.2020.9250908.

UVVM (Universal VHDL Verification Methodology)

https://www.uvvm.org/

Espen Tallaksen (EmLogic) and Marius Elvegård (Inventas). “Universal VHDL Verification Methodology (UVVM) Extension”. TEC-ED, TEC-SW & MB4SE OSIP Campaign Final Presentation Days - Spring 2022

UVM (Universal Verification Methodology) for ESA IP Cores

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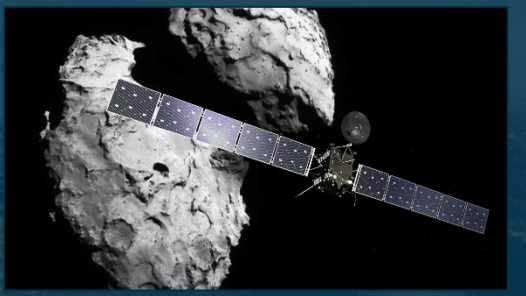
3. **Working at/with ESA**

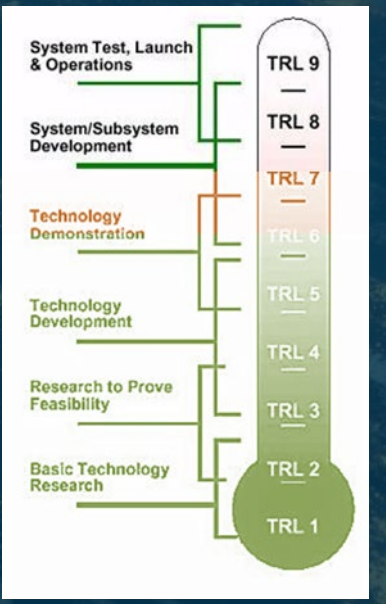


3. Working at/with ESA

Domains for *Computing Engineers*, all sorts of expertise are interesting, as might be:

- Ground segment/flight segment SW
- Digital electronics
- Architecture and Data-Handling
- uElectronics (FPGAs & digital/mixed-signal ASICs)
- System engineers

Technology Readiness Levels



Roles:

- Student Internship Programme
- Postgraduate positions MSc./PhD
- Professionals
- MSc./PhD. research stays

Collaborations with companies/universities:

- ESA programmes (**TDE**: TRL 1-4, **GSTPs**: > TRL 3..):
- **OSIP**: the Open Space Innovation Platform (Campaigns vs. Channels; Types: co-funded research, studies, early tech. development activities)

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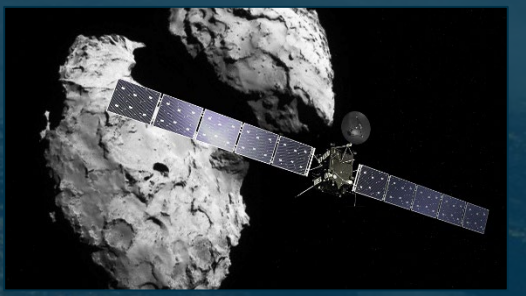
4. Q&A



4. Q & A

Any Questions!??

Thank you!