



Work stealing scheduling for performance portability of algorithms on parallel architectures

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resumen:

The goals of this presentation is to give both a brief overview of the research actions of my group at INRIA and a more deeper presentation on the scheduling of application by work stealing for parallel architecture.

In this presentation, I will illustrate some of works about the development of a runtime and an API for high performance computing for grid, cluster and multi-core architecture. The basic idea is to separate the description of the parallelism at the application level from the number of CPUs only known at runtime. I will focus on work stealing algorithms which permit theoretically efficient schedule on heterogeneous architectures and to obtain high performance on real architectures. I will present you how we have implemented a work stealing algorithm to schedule tasks with data flow dependencies. In order to reduce overhead at fine grain (~ order of magnitude of an empty C function call), I will introduce two technics: integration of work stealing scheduling decisions into the algorithm to allows lazy task creation; and a cooperative work stealing implementation based on atomic registers only. Both these technics outperform data parallel algorithms (transform, partial_sum, sort, count_if, ...) provides with Intel TBB, Cilk, MCSTL (parallel STL within GNU G++). Several experimentations on grid and multiprocessors will illustrate the presentation.

sobre Thierry Gauthier:

Dr. Thiery Gautier is a full time researcher at the INRIA French National Institute on Computer Science and Control. He earned his Dipl. Ing. M.S. and Ph.D. (1996) in computer science at the INPG, Grenoble, France. Dr. Gautier conducts research in high performance computing and has been involved with the design of fault tolerant protocols. He has lead the development of the Kernel for Asynchronous and Adaptive Interface KAAPI, which is fundamental to this research. He held in post-doctoral position at ETH Zürich (1997).