

Making the most out of Heterogeneous Chips with CPU, GPU and FPGA

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Sala de Grados - Lunes 11 de Diciembre de 2017 - 16:30
Entrada libre hasta completar el aforo

Resumen:

Heterogeneous computing is seen as a path forward to deliver the energy and performance improvements needed over the next decade. That way, heterogeneous systems feature GPUs (Graphics Processing Units) or FPGAs (Field Programmable Gate Arrays) that excel at accelerating complex tasks while consuming less energy. There are also heterogeneous architectures on-chip, like the processors developed for mobile devices (laptops, tablets and smartphones) comprised of multiple cores and a GPU. This talk covers hardware and software aspects of this kind of heterogeneous architectures. Regarding the HW, we briefly discuss the underlying architecture of some heterogeneous chips composed of multicores+GPU and multicores+FPGA, delving into the differences between both kind of accelerators and how to measure the energy they consume. We also address the different solutions to get a coherent view of the memory shared between the cores and the GPU or between the cores and the FPGA.

Sobre Rafael Asenjo Plaza:

Rafael Asenjo obtained a PhD in Telecommunication Engineering from the U. of Malaga, Spain in 1997. From 2001 to 2017, he was an Associate Professor in the Computer Architecture Department, being a Full Professor since 2017. He collaborated on the IBM XL-UPC compiler and on the Cray's Chapel runtime. In the last five years, he has focused on productively exploiting heterogeneous chips. In 2013 and 2014 he visited UIUC to work on CPU+GPU chips. In 2015 and 2016 he also started to work on CPU+FPGA chips while visiting U. of Bristol. He has served as General Chair for ACM PPOPP'16 and as an Organization Committee member as well as a Program Committee member for several HPC related conferences (PACT'17, EuroPar'17, SC'15). His research interests include heterogeneous programming models and architectures, parallelization of irregular codes and energy consumption. He co-presented two TBB tutorials at both EuroPar'17 and SC17.