Facultad de Informática
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## Robustness and Reliability of Deca-Nanometer Designs: Models, Recipes and Open Issues.

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*entrada libre hasta completar el aforo*

### resumen:

With the continuous scaling of transistor dimensions, the reliability degradation of circuits has become an important issue. Negative bias temperature instability (NBTI), in particular, has emerged as the most critical issue in determining the lifetime of CMOS devices and circuits.

NBTI manifests itself as an increase over time of the pMOS threshold voltage, which causes a progressive increase of delay of a device, and in turn, of a circuit. This effect is particularly nasty, since it can be regarded as a time-dependent systematic variation. The amount of NBTI-induced degradation effect depends on several device (e.g., size), environmental (e.g., Vdd), and functional (e.g., signal probability) parameters, that represent potential knobs to control and bound NBTI effects.

In this talk, we will review the basics of NBTI, and discuss (1) practical high-level models for the NBTI effect, (2) architectural- and gate-level solutions for tackling these effects, and (3) some contexts in which NBTI is likely to be especially critical, and that are still open problems.

### sobre Massimo Poncino:

Massimo Poncino is a Full Professor of Computing Systems at Politecnico di Torino, Italy. His research interests include several aspects of design automation of digital systems, with particular emphasis on the modeling and optimization of low-power systems. He has coauthored over 200 journal and conference papers, as well as a book on low-power memory design. He is an Associate Editor of the IEEE Transactions on CAD, and a member of ACM SIGDA Low-Power Technical Committee.