Facultad de Informática
Universidad Complutense de Madrid

ANUNCIO DE CONFERENCIA

Evolution of Electronic Design Automation Tools and Algorithms

Prof. Maciej Ciesielski

University of Massachusetts, Amherst, USA

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entrada libre hasta completar el aforo

resumen:

The goal of this lecture is to discuss the evolution of Computer Aided Design (CAD) field and the development of Electronic Design Automation (EDA) tools used by semiconductor companies and EDA vendors. It will cover a 30-year period from early 1980s to 2010 with some historical notes on earlier background theories and ideas. We will discuss the origins and the development of CAD algorithms, stress the importance of mathematical models used, review design representations and data structures, and briefly review the state-of the art academic and industrial EDA tools.

The following topics will be discussed, each illustrated with mathematical models used.

- Physical synthesis
  - Placement and floorplanning. Global routing and detailed routing. Maze and channel algorithms.
- Logic synthesis
  - Two-level logic (PLAs). Multi-level logic (ASIC, FPGAs). Canonical representations and their application (K-maps, BDDs).
- High-level synthesis
  - Scheduling, allocation, and binding. Dataflow graph generation and optimization.
- Verification and validation
  - Formal verification (combinational, sequential). Satisfiability (SAT and SMT). Simulation.
- Mathematical models used in EDA
  - Graph theory. Mathematical programming (Linear, Quadratic, Dynamic). Boolean algebra, Linear algebra.

sobre Maciej Ciesielski

Maciej Ciesielski received the M.S. in Electrical Engineering from Warsaw Technical University in 1974, and Ph.D. in Electrical Engineering from the University of Rochester in 1983. From 1983 to 1986 he was a Senior Member of Technical Staff at GTE Laboratories, Waltham, MA, where he worked on silicon compilation and layout synthesis projects. In 1987 he joined the Department of Electrical and Computer Engineering at the University of Massachusetts, Amherst, where he is currently Professor and Associate Department Head. He teaches and conducts research in the area of electronic design automation, and specifically in high-level and logic synthesis, formal verification and design validation of digital systems. He is recipient of Doctorate Honoris Causa from the Université de Bretagne Sud, Lorient, France, in 2008. He is a senior member of the IEEE.