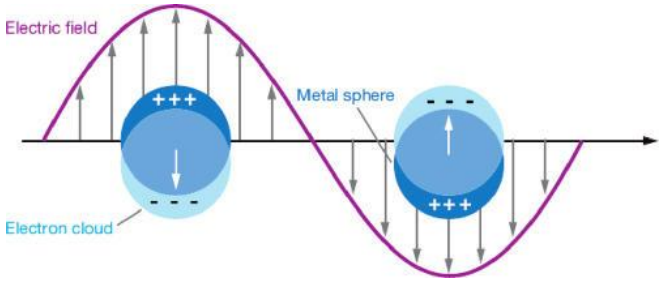
NANOSCALE CASCADED PLASMONIC LOGIC GATES FOR NON-BOOLEAN WAVE COMPUTATION

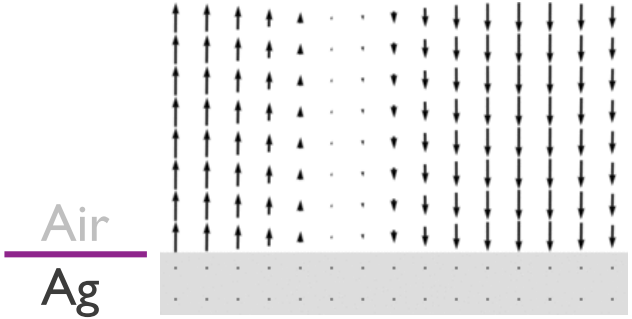
FRANCKY CATTHOOR AND PLASMONICS TEAM MEMBERS

INTRODUCTION OF PHYSICS PRINCIPLES

PLASMON, SP, SPP, SPPP, ...



Surface Plasmon Polariton



Source: wiki

Plasma
- Cloud of Free electrons: these oscillate!

Plasmon
- Quanta of plasma oscillation: these are collective!

Surface Plasmon (SP)
- Plasmon at interface (surface): M/D

Surface Plasmon Polariton (SPP)
- Quasiparticle
- Combination of light + SP

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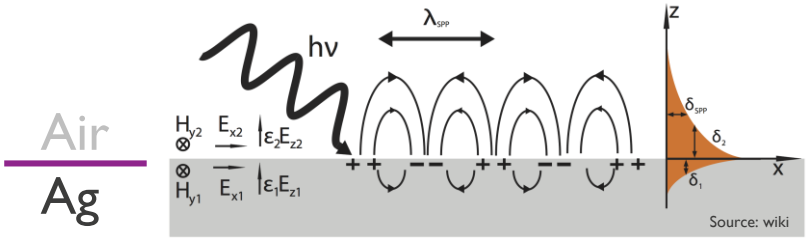
Surface Plasmon "Phonon" Polariton (SPPP)

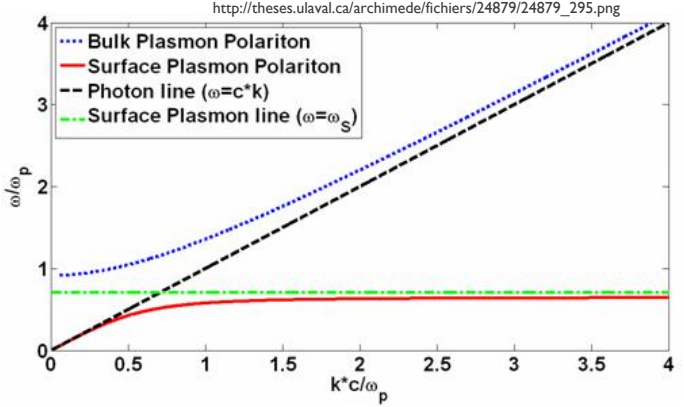
WHAT IS PLASMONICS?

Plasmonics is the study of the interaction between electromagnetic field and free electrons in a metal. -wiki



skin depth, k_{sp} and confinement

http://theses.ulaval.ca/archimede/fichiers/24879/24879_295.png



For a given wavelength of excitation, SPP wavelength is smaller: Squeeze Effect!
Optical Frequencies with a smaller wavelength: light on a wire!

TEAM

STRONG COLLABORATION WITH SEVERAL UNIV GROUPS

- IMEC: Francky Catthoor, PhD Surya Gurunarayanan, Odysseas Zografos, Dennis Lin, Pol Van Dorpe, Iuliana Radu, Bart Soree;
- Georgia Tech : PhDs Sourav Dutta, Dr. Chenyun Pan, PhD Samantha Lubaba Noor, Prof. Azad Naeemi
- EPFL: PhD Eleonora Testa, Dr. Matthias Soeken, Prof. Nanni De Micheli
- KULeuven-MICAS: PhD Kristof Dens, Prof. Patrick Reynaert

WHICH WAVE PHENOMENON TO START FROM?

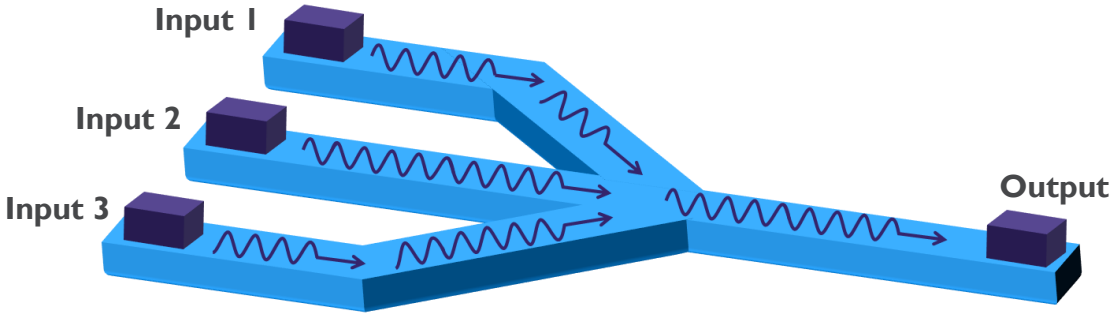
WAVE-BASED COMPUTING

MAIN CHARACTERISTICS WE WANT

- Spin waves and plasmonics have common feature – wave based computing
- Phase as a state variable – logic "1" and "0" encoded in the phase of the wave
- Exploit interference of the waves
- Inherent feature – majority voting due to interference which provides new way of combining boolean and non-boolean logic
- But also other very non-conventional logic wave functions can be created

INTRODUCTION TO PLASMONIC LOGIC

HOW DOES WAVE COMPUTATION WORK?



In wave computing, information is coded in the phase or the amplitude of the wave.

Computation by interference
Majority logic gate

I1	I2	I3	O
0	0	0	0
0	0	1	0
0	1	1	1
1	1	1	1

Output phase after interference is equal to the majority of input phases.

Different waves and physical state variables can be used.

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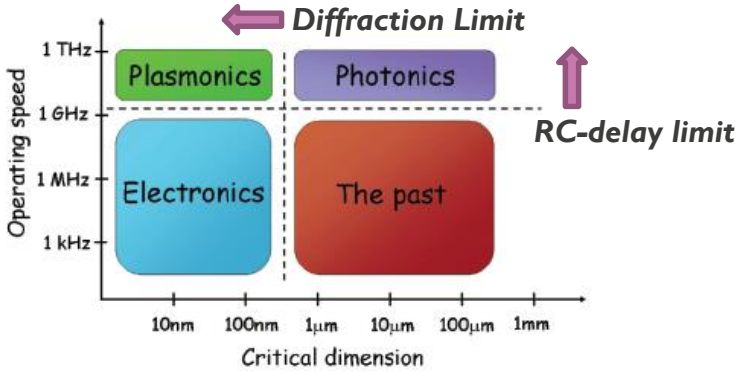
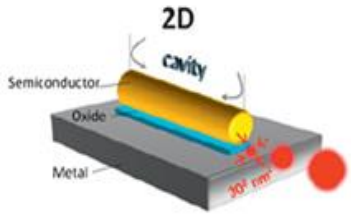
NEED FOR PLASMONICS

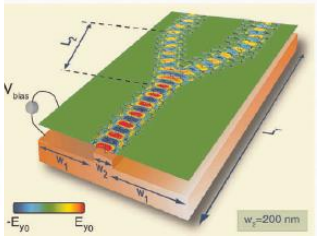


The size of electronics with speed of photonics!

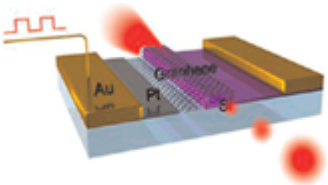
Sub-wavelength confinement:
Large field enhancements!



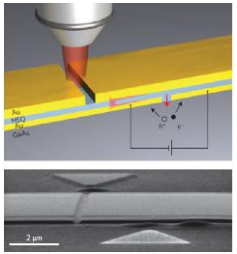
Emitters



Waveguides



Modulators



Detectors

Plasmonics: the next chip-scale technology, Rashid Zia, Jon A. Schuller, Anu Chandran, Mark L. Brongersma 2006

WAVE COMPUTING PARADIGMS

COMPARISON OF MAIN OPTIONS EXPLORED

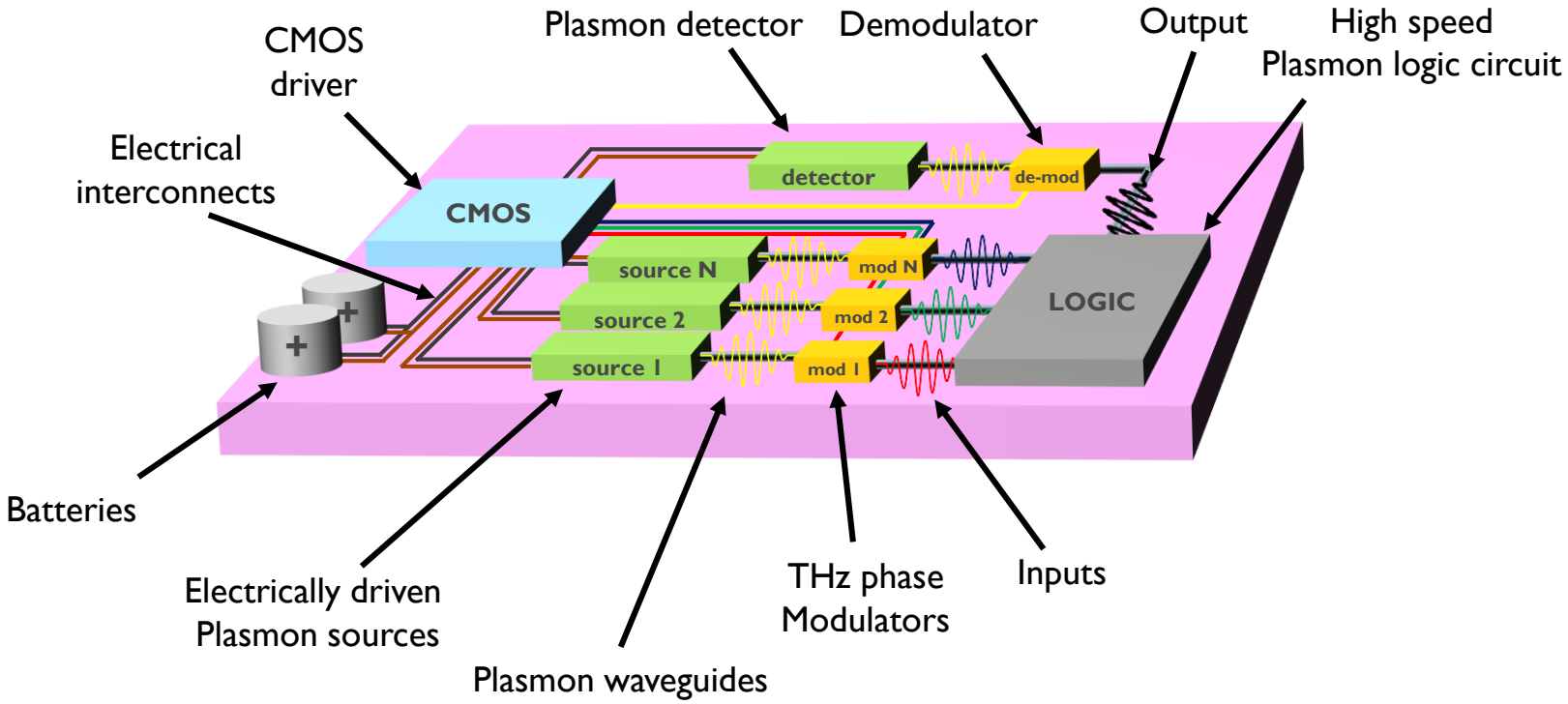
Property	Spin waves Magnons	Plasmons
Area/gate	🙂	☹
Gate Energy	🙂	😐
Overhead Energy	?	?
Delay-latency	☹	🙂🙂
Throughput	😐	🙂

Overall area and energy per function is likely better with plasmonics

The above should be reached without going to too high speed (>> THz) in/out bottleneck that dominates everything (which happens in photonic computing!)

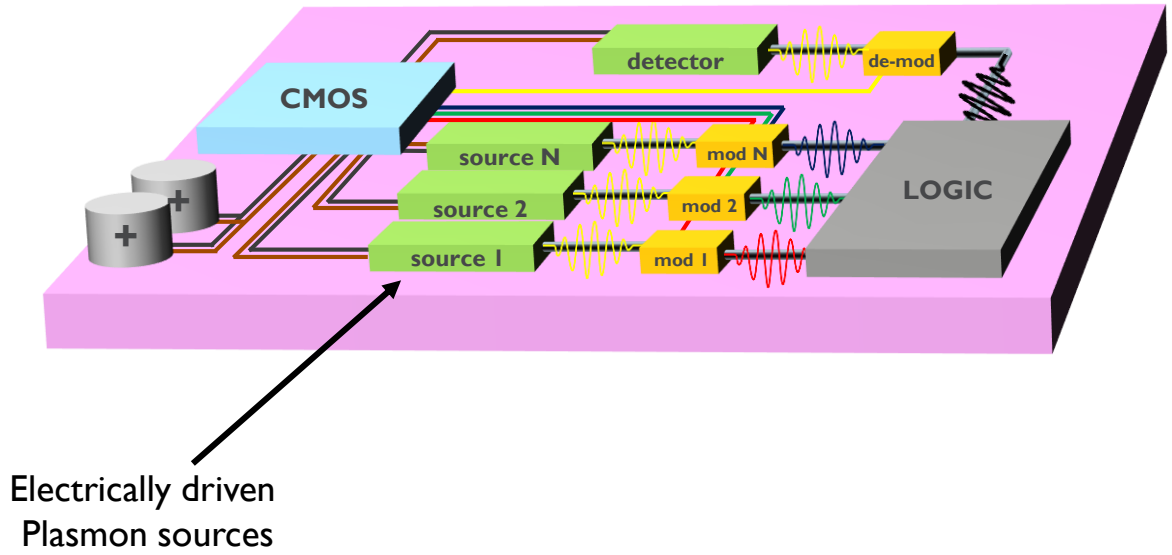
ON-CHIP PLASMONIC LOGIC

THE BIG PICTURE



ON-CHIP PLASMONIC LOGIC

EXCITATION (PHD OF SURYA GURUNARAYANAN)



PLASMON SOURCES

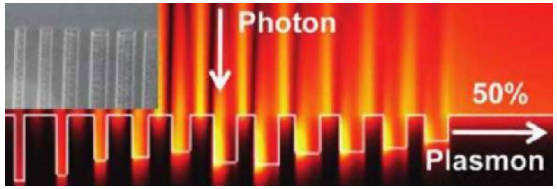
Two types: Optical & Electrical

1. Laser (optical) or STM tips (electrical)
Fast, but external schemes

2. On-chip semiconductor based LEDs
Locally emit light which excites plasmons.
Recombination limited → slow (~ns)

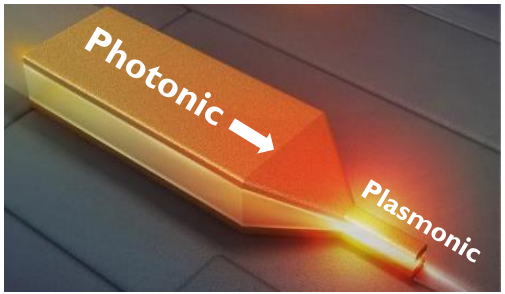
3. Tunneling:
~Instantaneous → promising

Optical External (Laser)



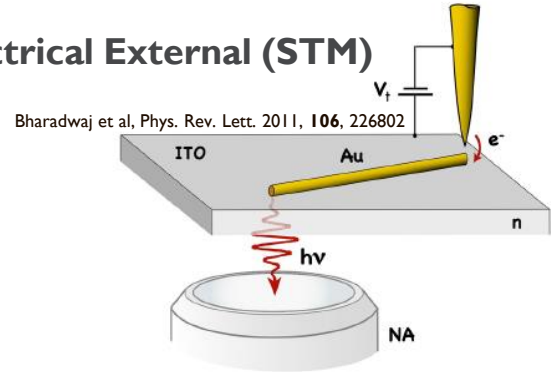
Zhao et al., EPJ Appl. Metamat. 2014, 1, 6

Optical Internal (3D taper)

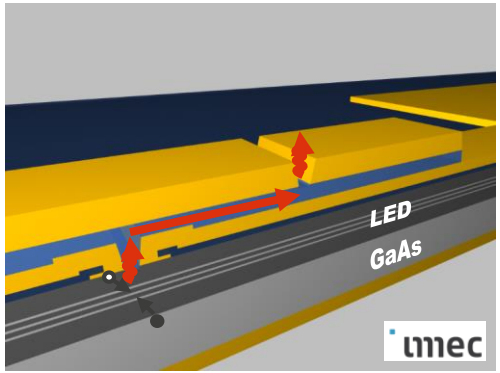


Choo et al, Nature Photonics 6, 838–844 (2012)

Electrical External (STM)



Electrical Internal (LED)



Neutens et al, Nano Lett. 2010, 10, 1429–1432

Tunneling is promising, need on-chip solution!

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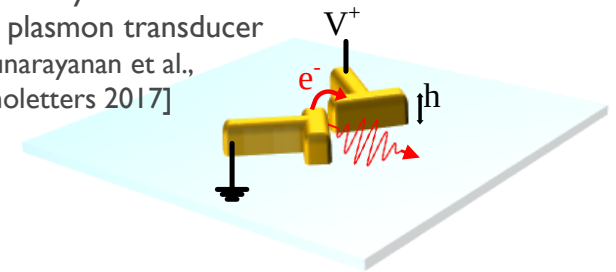
PLASMON SOURCE (ELECTRICAL)

On-chip voltage-based directional emitter

- Actively working on on-chip plasmon source
- First working prototype designed and developed at imec.
- Transducer from Electrical to Plasmon domain
- Ultra-fast (ps) and ultra-small (~100nm)

Electrically driven directional plasmon transducer [Gurunarayanan et al., Nanoletters 2017]



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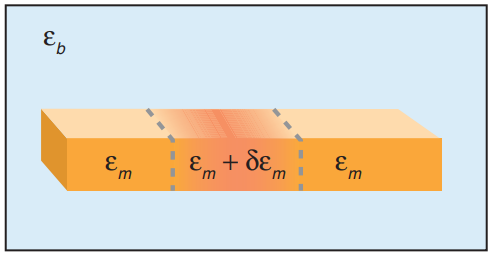
On-chip electrical plasmon source demonstrated.

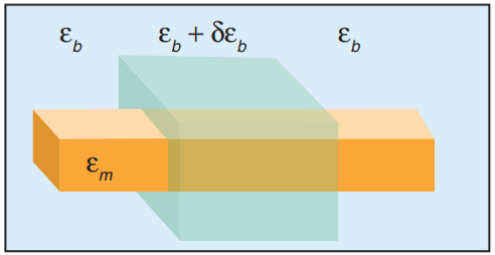
PLASMON PHASE MODULATORS

Information encoding in the phase

Modulation of metal permittivity



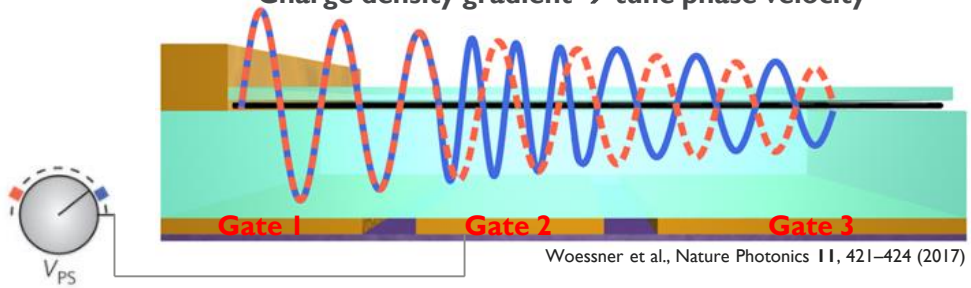
Modulation of background dielectric



Possible schemes: Electrical, mechanical, optical or thermal

- No ultra-small solutions exist!
- Requires further research.

2π phase change over 350nm
Graphene flake electrically modulated with 3 gates:
Charge density gradient → tune phase velocity



Woessner et al., Nature Photonics **11**, 421–424 (2017)

More research required!

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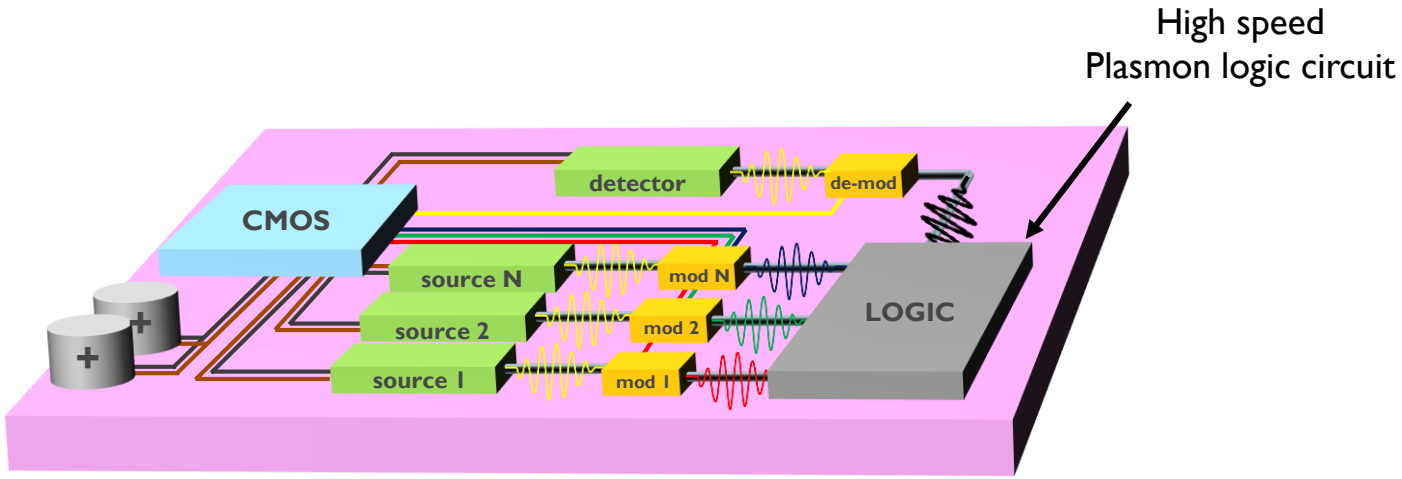
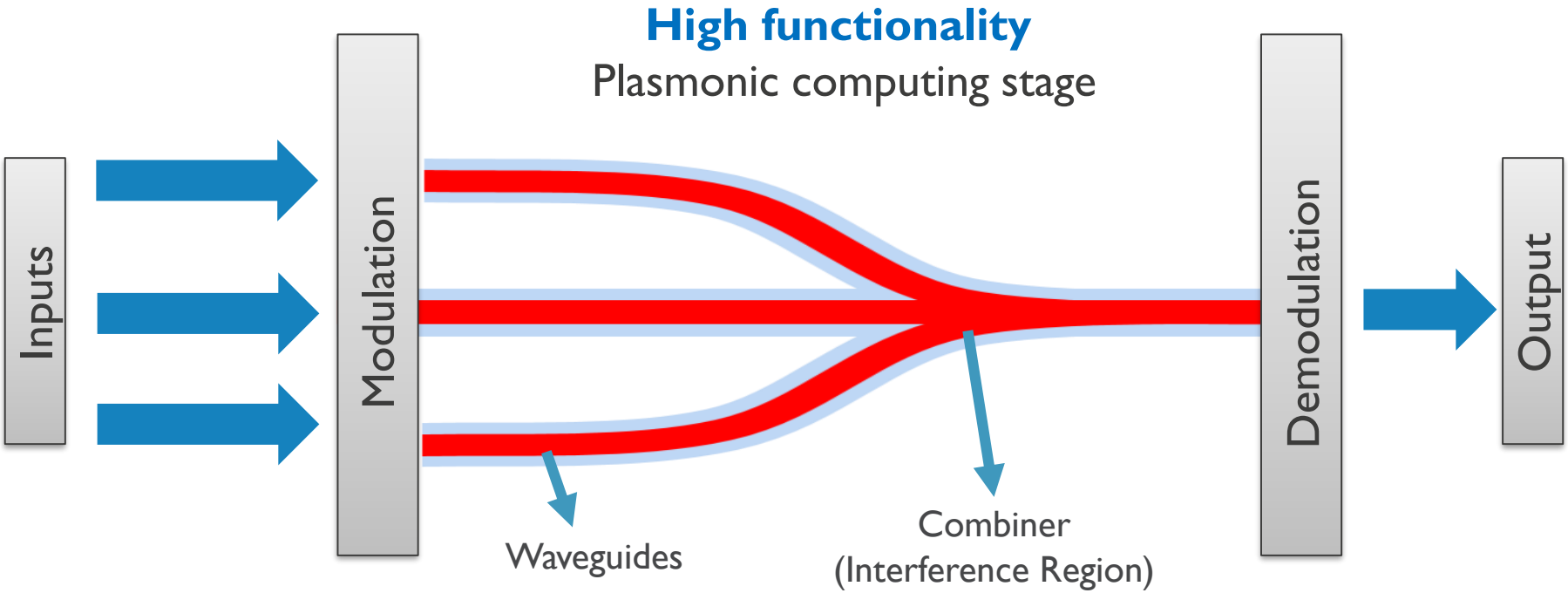
ON-CHIP PLASMONIC LOGIC

THE BIG PICTURE



WAVE COMPUTING WITH PLASMONS

Interference based ultra-fast computing



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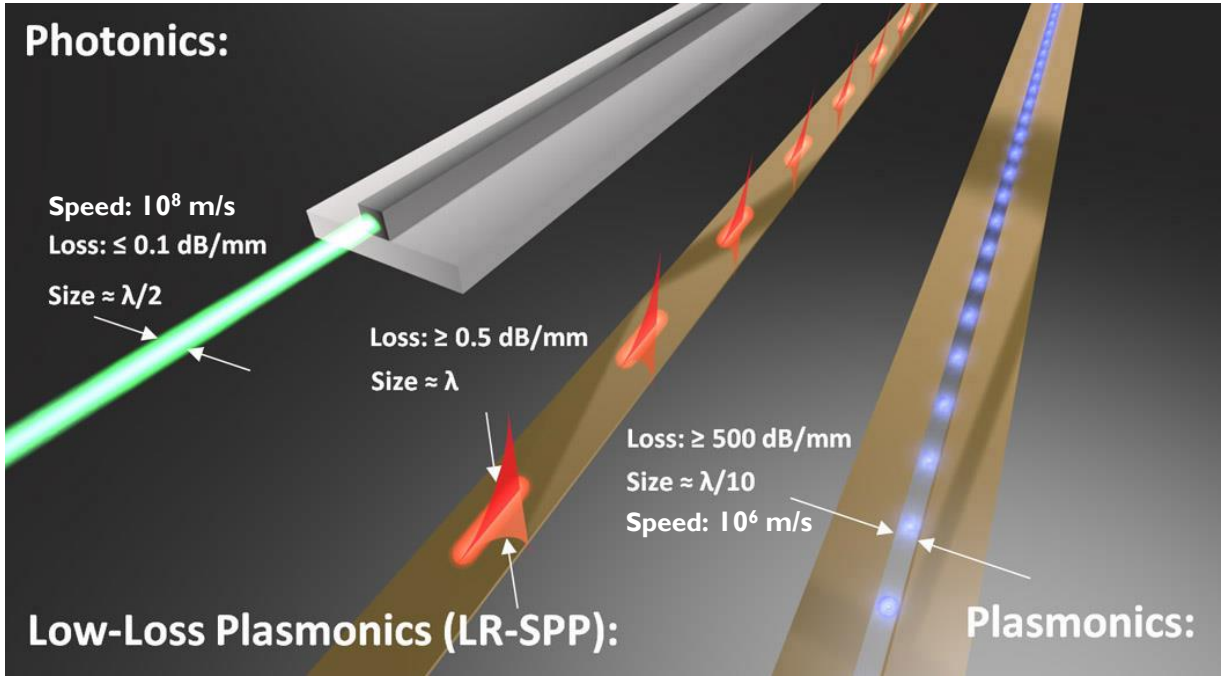
WAVEGUIDE COMPOSITION AND MATERIAL STACK EXPLORATION

PLASMON WAVEGUIDES

Comparison with photonic waveguide



Scale down size without compromising throughput

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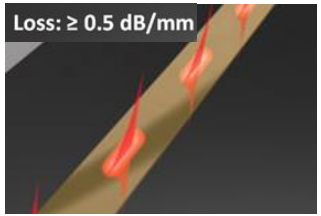
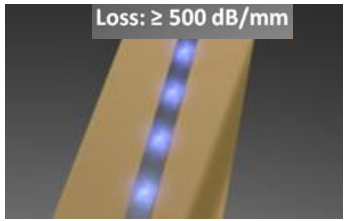
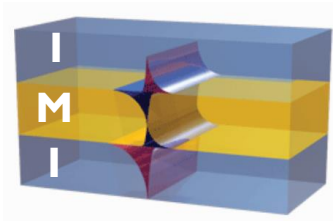
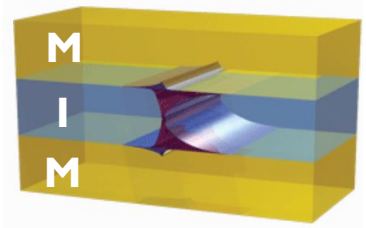
PLASMON WAVEGUIDES

Two basic flavors : IMI & MIM

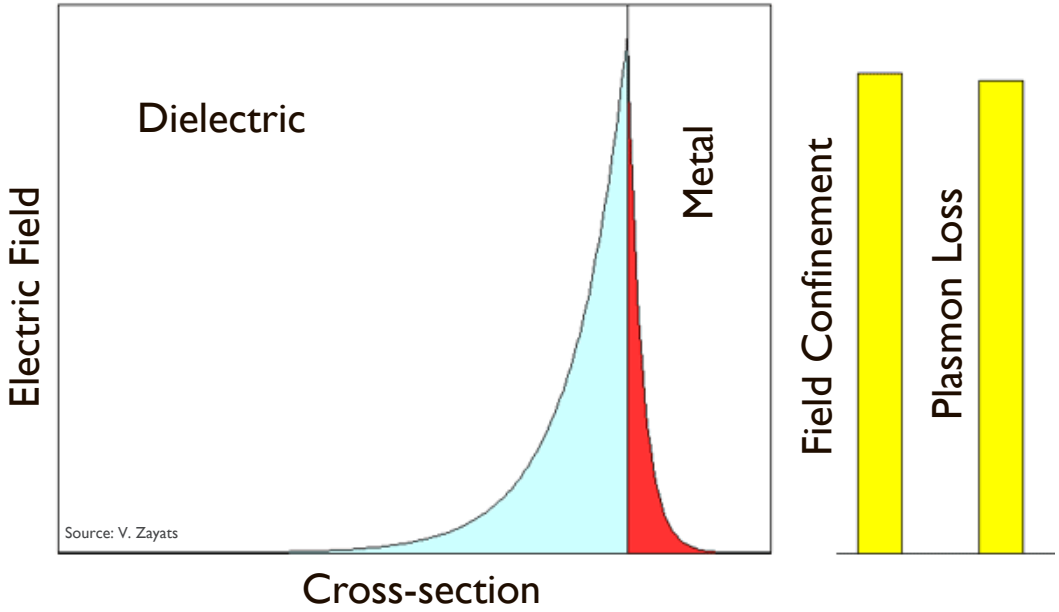








Low confinement **High confinement**



- IMI configuration is better suited for long propagation → plasmon interconnects
  - Low confinement → Large pitch
- MIM configuration is better suited for logic → strong confinement → small size → small pitch

MIM configuration is better suited for logic

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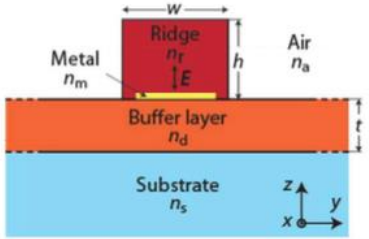
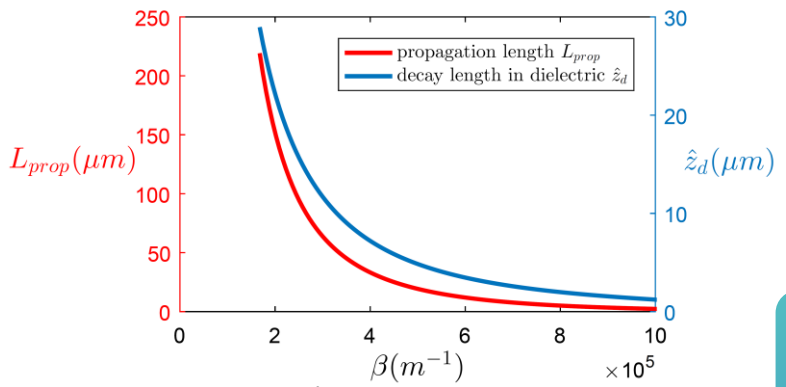
BASIC MATERIAL STACK FOR WAVEGUIDE: IMI



Explore waveguide stack options concl:
IMI or MIM easiest to start from

TRADE-OFF BETWEEN PROPAGATION LENGTH, CONFINEMENT AND GROUP VELOCITY IN IMI

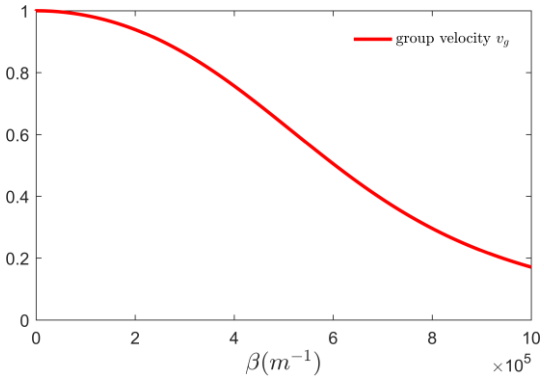
Trade-off propagation length and confinement



Small β:Propagation length in x good
But bad confinement in y-z direction
So λSPP ~1um for good Lprop (too) large

=> min pitch is also (too) large

Group velocity (norm. by speed of light c)



For larger propagation constant β

- Better y confinement (inverse with decay length) → denser packing of wires and devices ☺
- Smaller propagation length L_{prop} → less cascading and more E loss ☹
- Lower group velocity v_g → higher delay ☹

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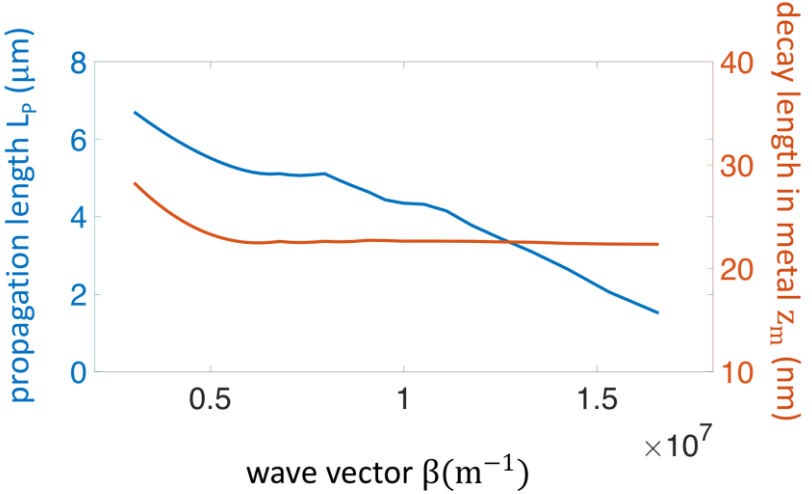
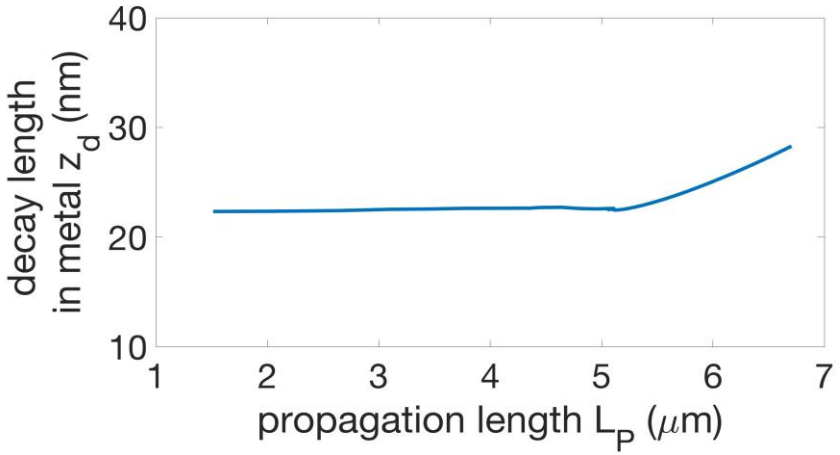
Ref: MSc thesis Jonas Doevenspeck'16 and j.paper:
Design and simulation of plasmonic interference-based majority gate
AIP Advances 7, 065116 (2017); doi: http://dx.doi.org/10.1063/1.4989817

BASIC MATERIAL STACK FOR WAVEGUIDE: MIM CASE





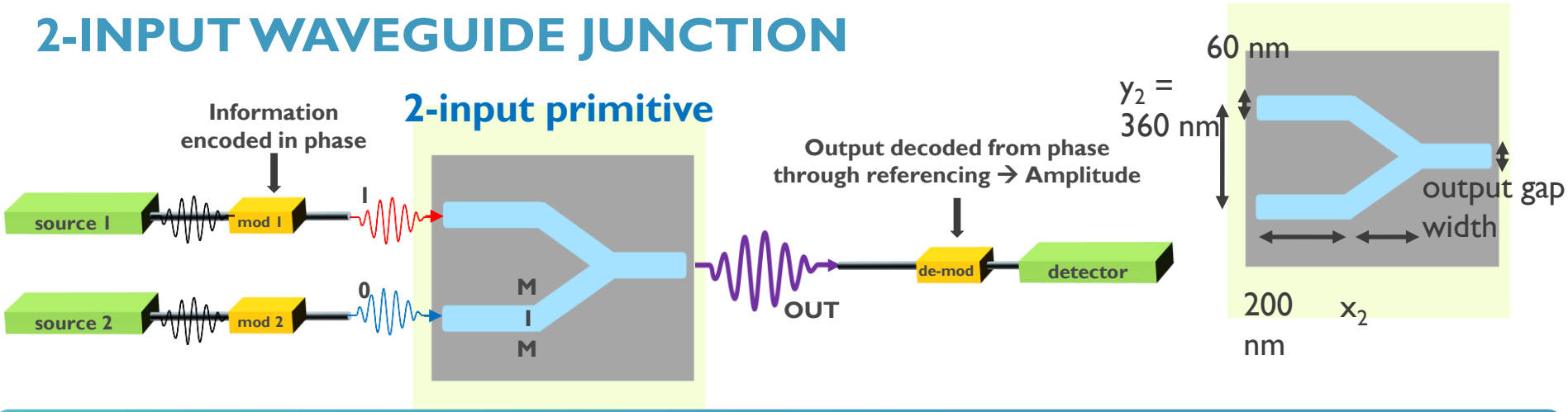
Propagation length in x direction is medium (few um)
But good confinement in the y direction
Selected λSPP ~860 nm is still high but the metal sides of the MIM waveguide determine the actual y-confinement (decay length)

=> min pitch is small (100s of nm)

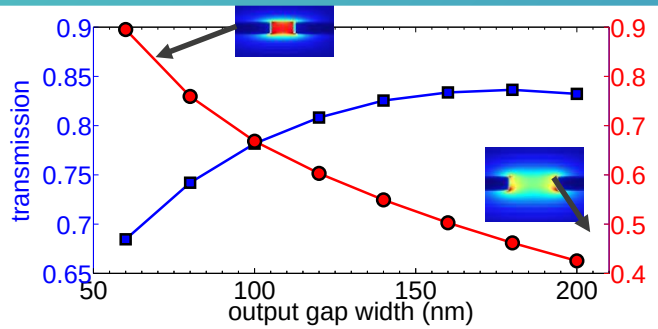
Ref: PhD thesis Sourav Dutta @ Georgia Tech and j.paper:
Proposal for nanoscale cascaded plasmonic majority gates for non-Boolean computation
Nature Scientific Reports, to be published

FROM MATERIAL STACK TO WAVEGUIDE JUNCTION AND LOGIC GATE

2-INPUT WAVEGUIDE JUNCTION

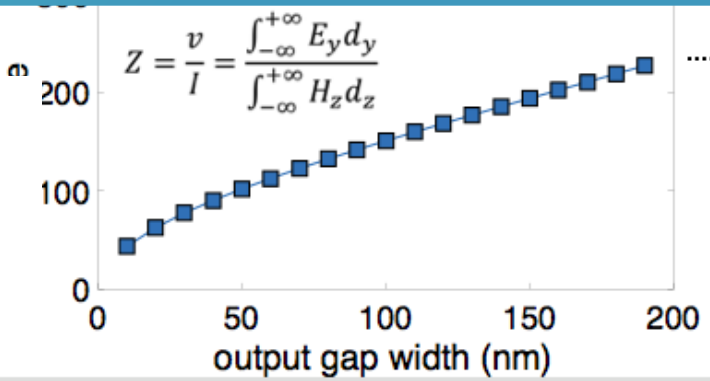


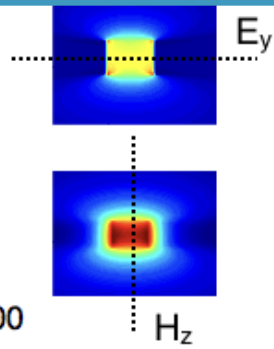
Trade-off between ease of detectability and transmission leads to good width/size



Normalized integrated electric field intensity

match

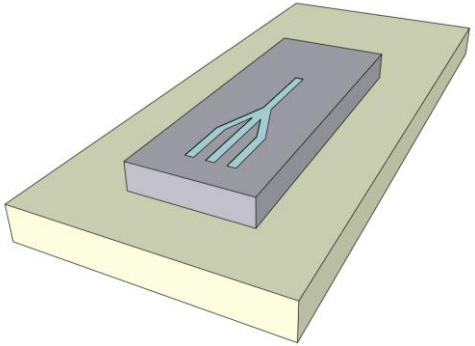




Ref: PhD thesis Sourav Dutta @ Georgia Tech and j.paper: Proposal for nanoscale cascaded plasmonic majority gates for non-Boolean computation. Nature Scientific Reports, to be published

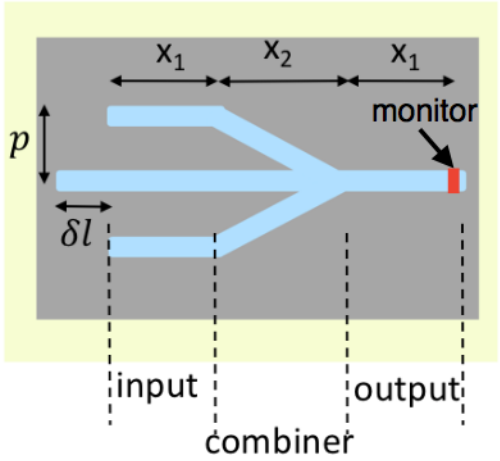
Ref: Cai, W., Shin, W., Fan, S. & Brongersma, M. L. Elements for Plasmonic Nanocircuits with Three-Dimensional Slot Waveguides. *Advanced materials* **22**, 5120-5124 (2010).

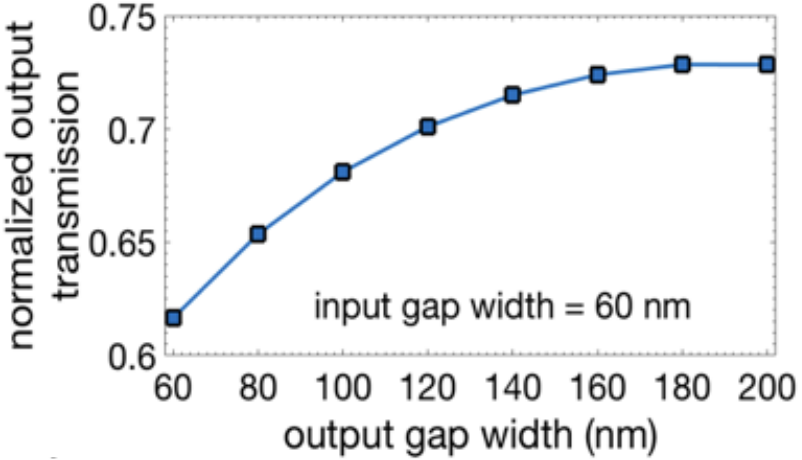
3-INPUT LOGIC GATE



p = 360 nm

60 nm





(a)

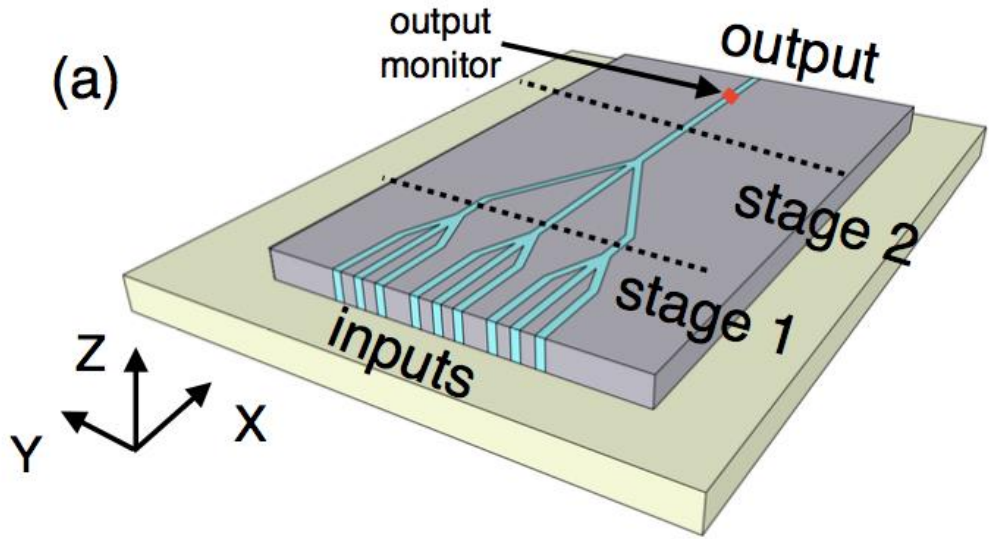
Also for 3-input waveguide dimensions stay reasonable
But gate pitch grows (2*360 nm)

Ref: PhD thesis Sourav Dutta @ Georgia Tech and j.paper:
Proposal for nanoscale cascaded plasmonic majority gates for non-Boolean computation
Nature Scientific Reports, to be published

25

CASCADING STAGES TO CREATE RELEVANT CIRCUITS

2 STAGE CASCADED LOGIC GATES



Stage1 width= 60 nm
Stage2 width= 120 nm

Simple way of cascading (as opposed to e.g. spin waves in earlier session)

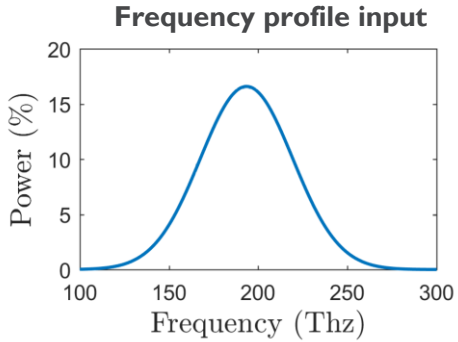
INPUT WAVEFORM ILLUSTRATION

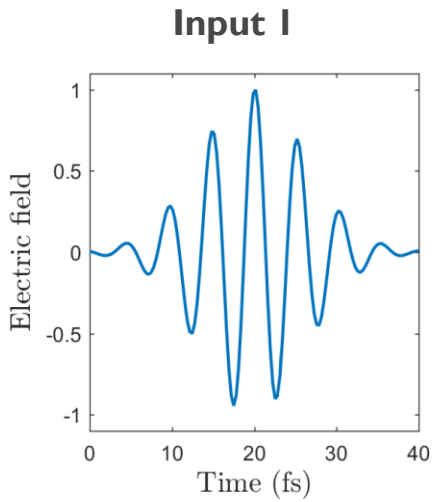
PHASE CODING-MODULATION

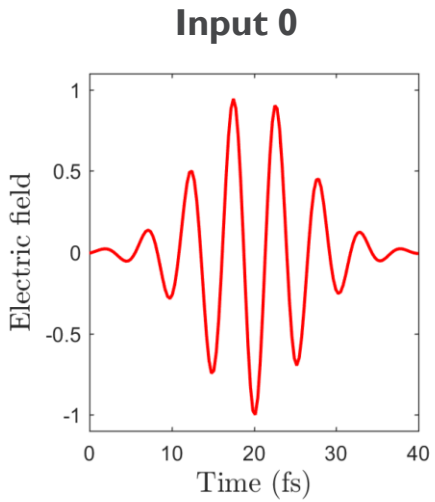
Example input: 1550 nm wave → 193 Thz
40 fs pulse width

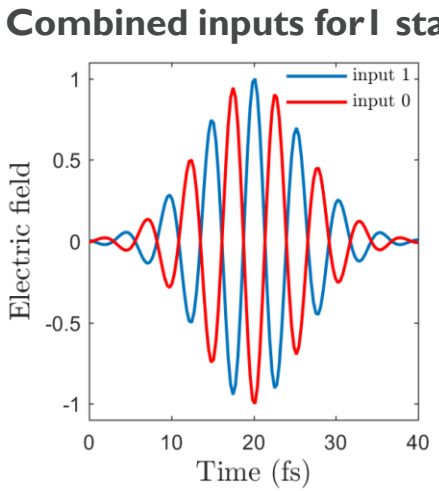
Input '1' and '0' phase difference of π

Simple way of modulating (as opposed to amplitude modul.)









Electric field normalized to maximum E-field from source

Ref: MSc thesis Jonas Doevenspeck'16 and j.paper:
Design and simulation of plasmonic interference-based majority gate
AIP Advances 7, 065116 (2017); doi: http://dx.doi.org/10.1063/1.4989817

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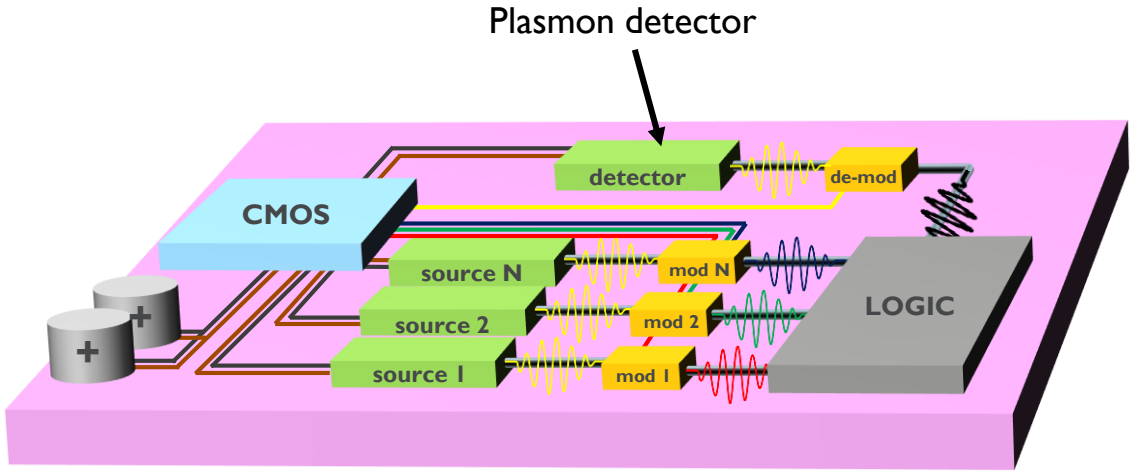
ON-CHIP PLASMONIC LOGIC

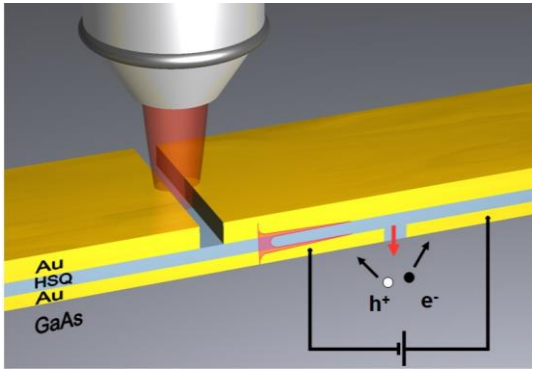
THE BIG PICTURE



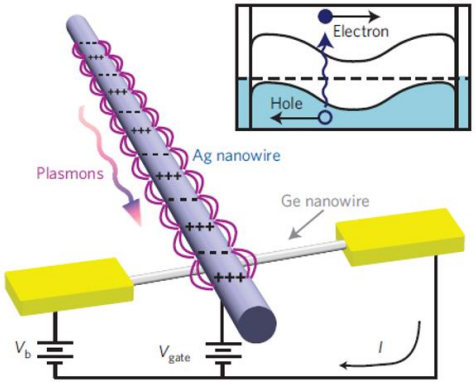
ON-CHIP PLASMON DETECTORS

Semiconductor or tunneling based

1. Semiconductors



Neutens et al., Nature Photonics 3, 283–286 (2009)

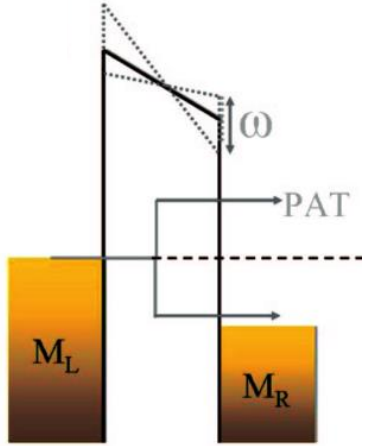


Falk et al., Nature Physics 5, 475–479 (2009)

1. Plasmon excites electron-hole pair in the semiconductor.
2. Carriers generate photocurrent

Drift/diffusion limited ➔ slow (ns to µs)

2. Tunneling/Ballistic transport

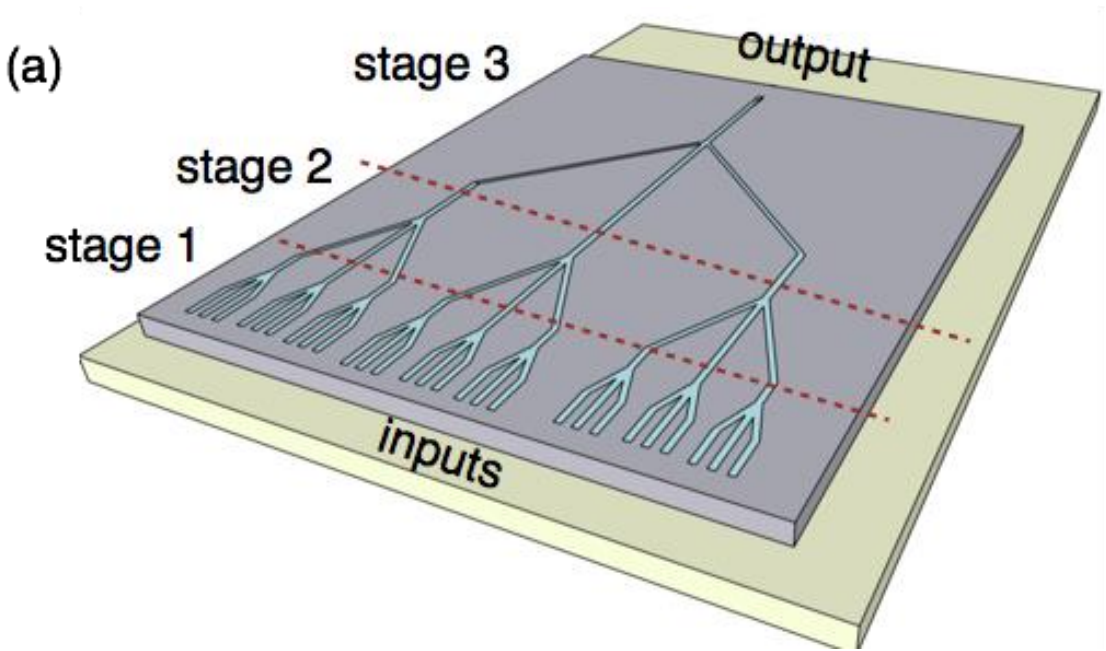


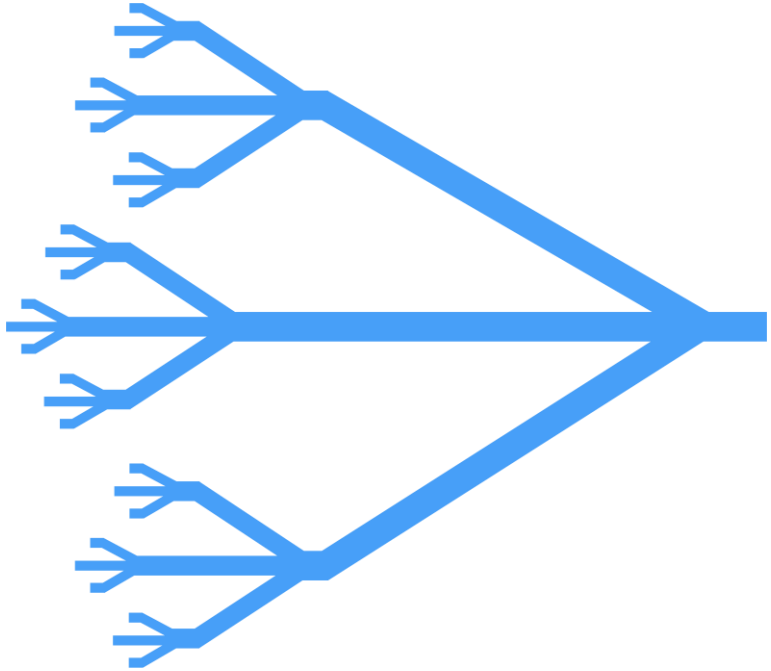
Ittah et cl., NANO LETTERS 2009 Vol. 9, No. 4 1615-1620

- Oscillating field at the junction results in photon-assisted transport.
- Also works for plasmon-assisted tunneling transport
- Very fast: ~ps

On-chip ultra-fast solution ➔ tunneling based transducers!

3 STAGE CASCADED LOGIC GATES





Gradually widening gap/spacing but pitch remains reasonable (few um)

Ref: PhD thesis Sourav Dutta @ Georgia Tech and j.paper:
Proposal for nanoscale cascaded plasmonic majority gates for non-Boolean computation
Nature Scientific Reports, to be published

MAPPING OF REALISTIC CIRCUIT FUNCTIONALITY

REAL PROOF-OF-THE-PUDDING COMES FROM FUNCTIONS!

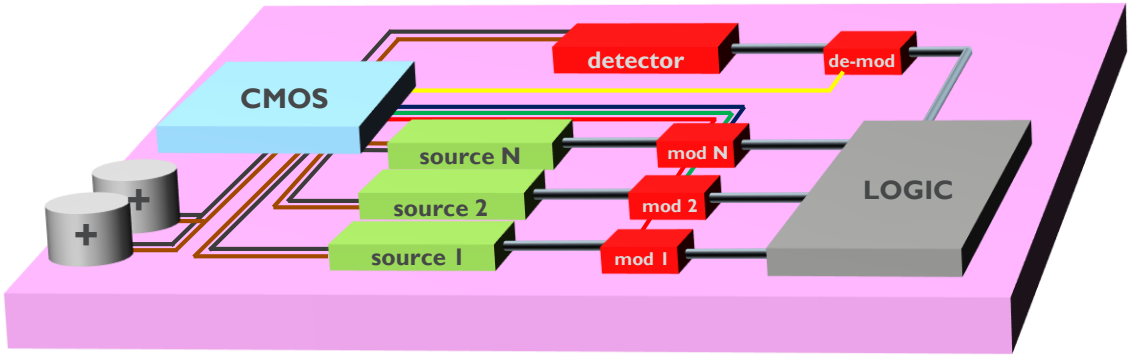
- This requires access to plasmonics oriented mapping and synthesis tools because pen-and-paper/excel type studies do not incorporate the strongly non-linear and correlated nature of realistic function mapping.

- We are actively busy with this exploration in tight cooperation with EPFL and early results are promising

PLASMONIC LOGIC – SUMMARY

- Very interesting results from proof-of-principle experiments:
  1. On-chip directional plasmon source is realized for the first time.
  2. Exploration study of plasmonics waveguides supports feasibility of wave-based computing
  3. Plasmonic Majority gate + cascadability up to 3 stages is shown.

- Challenging but exciting road ahead:
  - ❑ Experimental realization of majority logic
  - ❑ Build high-level logic design elements:
    - Logic synthesis mapping



Legend

- Work in progress
- Simulations, demonstration required
- Future work

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REMAINING CHALLENGES

- Referencing output for changing the state variable from phase to amplitude allows realistic detection mechanism. Still requires low power THz range electronic detector but we have started investigation into that + collaboration planned
- Also need for effective low power plasmon stimulator: active exploration ongoing
- Mapping/synthesis framework should be adapted: we are actively collaborating on this