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eNVM based data and instruction memory hierarchy for ulta-low power data-parallel processor platforms

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entrada libre hasta completar el aforo

resumen:

Scaling of volatile SRAM and DRAM memories is hitting limits on read and write power, area and endurance/reliability characteristics. For that reason, several researchers have started to study alternatives based on embedded non-volatile memory (eNVM) options such as magnetic STT-MRAMs or domain wall RAMS and resistive ReRAMs. These are very promising in terms of reducing leakage and area, and indirectly also the dynamic read power. But they are not meeting the write speed requirements and partly also endurance/reliability can be an issue. Hence, they have an impact on the choices made in the memory organisation. Potentially they can replace the lower layer memories in both the instruction and the data hierarchy but with some changes to mitigate the write latency and endurance/reliability aspects. In this talk a few interesting directions will be highlighted, including the embedding in a complete data-parallel processor platform.

Sobre Francky Catthoor:

Prof. Francky Catthoor is a fellow at IMEC, Heverlee, Belgium. He received the Eng. degree and a Ph.D. in El. Eng. from the K.U.Leuven, Belgium in 1982 and 1987 respectively. Since 1987, he has headed research domains in the area of architectural and system-level synthesis methodologies, within the DESICS (formerly VSDM) division at IMEC. His current research activities belong to the field of architecture design methods and system-level exploration for power and memory footprint within real-time constraints, oriented towards data storage management, global data transfer optimization and concurrency exploitation. Platforms that contain both customizable/configurable architectures and (parallel) programmable instruction-set processors are targeted.