Facultad de Informática
Universidad Complutense de Madrid

ANUNCIO DE CONFERENCIA

Online Management of Unpredictably Heterogeneous Multi-core Microprocessors.

Prof. David H. Albonesi

Associate Professor, Computer Systems Laboratory. School of Electrical and Computer Engineering, Cornell University, USA.

Sala de Grados • 18 de marzo de 2009 • 12: 00
entrada libre hasta completar el aforo

resumen:

In future large-scale multi-core microprocessors, hard errors and process variations will create unpredictable heterogeneity, in which the cores vary in their performance and power characteristics in an unanticipated manner. Under this scenario, conventional power management and thread scheduling techniques may cause large performance losses and power inefficiencies. We propose a new coordinated power management and thread scheduling approach that accounts for this uncertainty in core characteristics. The power manager leverages on-chip regulators with fast switching rates by assigning each core a fraction of the overall chip power budget, which gives each core the freedom to meet its budget through local voltage/frequency control. The scheduler simultaneously factors in both performance and power objectives by extrapolating what decisions the power manager would make when presented with a particular scheduling assignment. In this manner, the scheduler works synergistically with the power manager to achieve the best throughput under a given power constraint. The combined scheme automatically adjusts to changes in frequency, leakage power, and hardware functionality over the lifetime of the chip.

sobre David H. Albonesi:

David Albonesi is an Associate Professor in the School of Electrical and Computer Engineering at Cornell University and a member of the Computer Systems Laboratory. Prior to joining Cornell in 2004, he spent eight years as a faculty member at the University of Rochester, and ten years in design and management in the computer industry. His research group investigates adaptive, power-efficient, and reliability-aware computer architectures, and multicore architectures exploiting new technologies.