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COTSon: Infrastructure for system-level simulation.

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resumen:

HP Labs' COTSon simulator based on AMD's SimNow is a full system simulation infrastructure. It allows to simulate complete systems ranging from multicore nodes up to full clusters of multicore nodes with complete network simulation. It is composed of a pluggable architecture, in which most features can be substituted for your own development, thus allowing researchers to use it as their simulation platform. There are tons of simulators, why a new one? COTSon is not just another simulator, it is a simulation infrastructure where you can plugin your own simulation modules. Our holistic approach simulates the whole system at once, because we believe that multicore multithreaded architectures of the future can not be understood without taking into account the whole system, including devices and the whole operating system. Something similar can be said about disk and network research. As a design principle, COTSon trades off accuracy for speed and viceversa, dynamically allowing the researcher to determine the interesting parts of their application, as well as doing large space explorations at higher speeds. Why use many tools if one suffices? We hope COTSon becomes the de facto standard simulation infrastructure for next generation systems simulation, and that is why we are making it freely available under request. If you belong to any kind of research lab or university and you are interested in microarchitecture simulation, disk simulation, network simulation or system simulation, COTSon may be perfect for you. In this talk, we provide a general description of COTSon and explain the different research challengues and solutions behind the development of our simulation infrastructure. More information about COTSon can be found at http://sites.google.com/site/hplabscotson.

sobre Daniel Ortega:

Daniel Ortega is a Senior Research Scientist at HP Labs. He joined HP in 2003 after finishing his PhD in Computer Architecture at the Universitat Politècnica de Catalunya (UPC). His current research interests include simulation and programming languages. He has previous experience in content processing systems, dynamic optimization, and computer architecture. He is an active member of the Computer Architecture community and has published more than 10 publications in journals and international conferences such as ISCA, HPCA, ISPASS and journals such as Operating Systems Review. He is involved in the community and has served as part of Technical Program Committees of both ISPASS 2008 and EuroPar 2008, and he was part of the organizing committee of the 5th HiPEAC Industrial Workshop. He has disclosed 13 patents.