Automatic generation of hardware memory architectures for HPC

Christian Pilato

Politecnico di Milano

Facultad de Informática

on line - meet.google.com/hin-hgxj-ide - jueves 21 de abril de 2022 - 17:00

Entrada libre hasta completar el aforo

Resumen:

Many HPC applications are massively parallel and can benefit from the spatial parallelism offered by reconfigurable logic. While modern memory technologies can offer high bandwidth, designers must craft advanced communication and memory architectures for efficient data movement and on-chip storage. Addressing these challenges requires to combine compiler optimizations, high-level synthesis, and hardware design. In this talk, I will present challenges, solutions, and trends for generating massively parallel accelerators on FPGA for high-performance computing. These architectures can provide performance comparable to software implementations on high-end processors, and much higher energy efficiency thanks to logic customization.

Sobre Christian Pilato:

Christian Pilato is a Tenure-Track Assistant Professor at Politecnico di Milano. He was a Post-doc Research Scientist at Columbia University (2013-2016) and at the ALaRI Institute of the Università della Svizzera italiana (2016-2018). He was also a Visiting Researcher at New York University, Delft University of Technology, and Chalmers University of Technology. He has a Ph.D. in Information Technology from Politecnico di Milano (2011). His research interests focus on the design, optimization, and prototyping of heterogeneous system-on-chip architectures and reconfigurable systems, with emphasis on memory and security aspects. Starting from October 2020, he is the Scientific Coordinator of the H2020 EVEREST project. He served as program chair of EUC 2014 and is currently serving in the program and organizing committees of many conferences on EDA, CAD, embedded systems, and reconfigurable architectures (DAC, ICCAD, DATE, CASES, FPL, ICCD, etc.) He is a Senior Member of IEEE and ACM, and a Member of HiPEAC.