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Protecting data and intellectual property in accelerator-rich architectures with high-level methods

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Resumen:

The globalization of the electronics supply chain allows for the reduction of chip manufacturing costs but poses new security threats. Untrusted foundries can steal the intellectual property in the chips, while malicious users can tamper with the systems to steal sensitive information. The design of next-generation systems requires to change the design methods, introducing security concepts since the early stages. In this talk, I will present an overview of the security issues in the design of accelerator-rich architecture, focusing on the protection of the data and the intellectual property. I will also discuss high-level methods to address these concerns, along with metrics for their evaluations. These solutions include the design and prototyping of architectures with secure communications, the high-level synthesis of security countermeasures, and the logic locking of RTL designs.

Sobre Christian Pilato:

Christian Pilato is a Tenure-Track Assistant Professor at Politecnico di Milano. He was a Post-doc Research Scientist at Columbia University (2013-2016) and at the ALaRI Institute of the Università della Svizzera italiana (2016-2018). He was also a Visiting Researcher at New York University, Delft University of Technology, and Chalmers University of Technology. He has a Ph.D. in Information Technology from Politecnico di Milano (2011). His research interests focus on the design, optimization, and prototyping of heterogeneous system-on-chip architectures and reconfigurable systems, with emphasis on memory and security aspects. Starting from October 2020, he is the Scientific Coordinator of the H2020 EVEREST project. He served as program chair of EUC 2014 and is currently serving in the program committees of many conferences on EDA, CAD, embedded systems, and reconfigurable architectures (DAC, ICCAD, DATE, CASES, FPL, ICCD, etc.) He is a Senior Member of IEEE and ACM, and a Member of HiPEAC.